HACETTEPE UNIVERSITY
Department of Computer Science and Engineering

BBM233 Logic Design Laboratory

EXPERIMENT 3
FLIP-FLOPS

AIM

In this experiment different types of flip-flops such as RS, JK and D flip-flops will be examined.

BACKGROUND

The logic circuits we encountered in Experiment 1 all have one thing in common. Their outputs at a given time are function only of their inputs at that time. Such circuits are called combinational logic circuits. This experiment and in fact, nearly all subsequent experiments deal with sequential circuits. The output of a sequential circuit is determined by its present inputs and by its internal state. In other words, a sequential circuit is a device with memory. Sequential circuits are made of flip-flops. There are three different types of flip-flops which are RS (Reset-Set), JK and D (Delay).

THE RS FLIP-FLOP

The smallest unit of information is binary digit or bit. As the simplest sequential circuit, the RS flip-flop is capable of storing only one bit of information. The RS flip-flop can be constructed using two NOR (or NAND) gate as shown in Figure 3.1. Note that the output of each gate is fed back to the input of the other gates. This feedback is an essential feature of all sequential circuits.

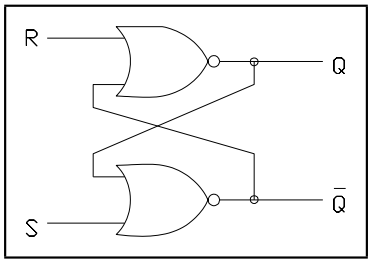

Figure 3.1 The RS flip-flop

If both inputs of the flip-flop are at state 0, the output Q either will be in state 1 or 0 (previous state). If S=1 and R=0, then Q=1. If S=0 R=1, then Q=0. The condition R=S=1 is not permitted. Thus, in order for the RS flip-flop outputs are functions strictly of the inputs.

The state of a flip-flop is represented by the value on its Q output. If the flip-flop initially is in state X (0 or 1) with both inputs equal to 0, then its behavior can be represented by the truth table shown below:

R	S	Q	Q/
0	0	Q	Q/
0	1	1	0
1	0	0	1
1	1	U	U

U: Undetermined.

The transition from the case of R=S=1 to R=S=0 is a condition. If R is set to 0 slightly ahead of S, the flip-flop will assume state 1 (Q=1); if S wins the race, state 0 (Q=0) results. The uncertainty is intolerable in a real system and so the situation S=R=1 should not be allowed to occur.

THE JK FLIP-FLOP

Another kind of flip-flop is JK flip-flop. A 7476 package contains two JK flip-flops. Figure 3.2 shows its truth table and pins configuration. PR and CLR pins are used to set (PReset) and CLeaR the flip-flop asynchronously. A JK flip-flop with J=K/ is called D flip-flop. A D flip-flop can be seen as a device with an input (D), an output (Q) and a clock (CLK).

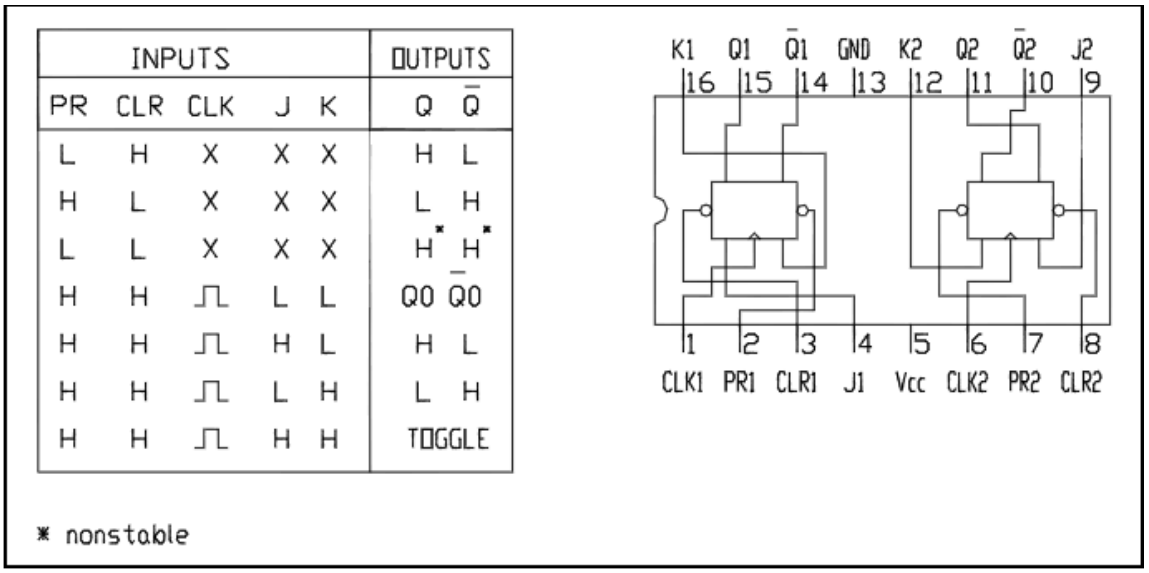

Figure 3.2 JK Flip-Flops

In many circuits, pulses with only a few nanoseconds of duration are produced at various points. Because JK flip-flops respond to extremely short pulses they can be used in order to detect the presence of such pulses. Thus, with J=K=1, a pulse on the clock input can be detected by a state change.

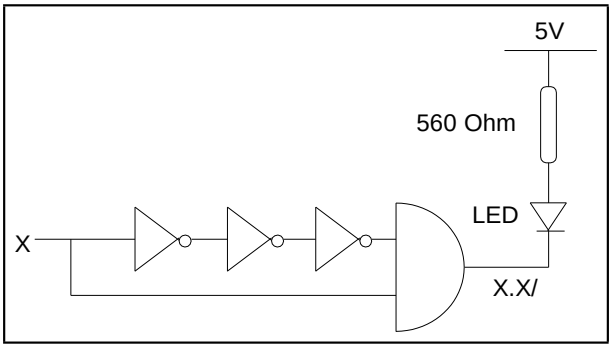

Figure 3.3 Short pulse generating circuit

For example, if the output of one of the toggled logic sources, denoted X, is passed through a string of three NOT gates shown in Figure 3.3, it is inverted to produce X/ and delayed by about 45 nanoseconds approximatively. Now since X.X/=0 regardless of the value of X, one might expect the output of an AND gate with X and X/ (not X) as inputs to be 0 at all times. In fact, the LED never goes off. Without a means of detecting short pulses, we cannot determine whether a pulse appears at the output of the AND gate or not. The Step 4 of the Experiment deals with this detection.

PREREQUISITE

- Implement JK flip-flop with Verilog on ISE.

EXPERIMENT

Before proceeding to the following Steps, please answer the two questions:

1. What is a sequential circuit? What is the difference between a synchronous sequential circuit and an asynchronous sequential circuit?
2. What is propagation delay?

STEP1 Implement the circuit of Figure 3.1 (The RS flip-flop) and become familiar with its operation.

STEP2 Implement an RS flip-flop using NAND gates. Determine its truth table. Which combination of inputs is illegal here? Explain.

STEP3 Using one of the JK flip-flops in the 7476 package and become familiar with its operation. For this purpose, connect its inputs to different voltage level, outputs to LEDs. The clock input should be connected to the signal generator with an appropriate frequency.

STEP4 Implement the circuit of Figure 3.3 and verify that the lamp remains always on. Feed the output of the AND gate into the clock input of the JK flip-flop of Step 3. Verify first if the JK flip-flop toggles.

COMPONENTS NEEDED

- A 7400 Quad 2-input NAND Gate
- A 7402 Quad 2-input NOR Gate
- A 7404 Hex Inverter
- A 7408 Quad 2-input AND Gate
- A 7476 Dual JK flip-flop
- LED
- Resistors