EXPERIMENT 6
DATA SELECTORS, DECODERS AND MEMORIES

AIM

In this experiment circuits such as Data Selectors, Address Decoders and Memories will be examined.

BACKGROUND

In digital systems where information from multiple sources must be processed, it is necessary to have circuits that provide selective access to them. Data selectors and address decoders are among such selection circuits.

DATA SELECTOR / MULTIPLEXER

A data selector is an integrated circuit with n inputs and an output. It permits one of the n inputs, to be switched to the output. The selection of the input to switch is done upon the code placed on the address lines. The 74151 is a data selector with 8 strobe inputs and complementary outputs. Figure 7.1 shows its connection diagram and truth table. The input STB must be at a low level to enable the device. A high level on this control input forces output W to high, and Y to low, independently of the inputs.
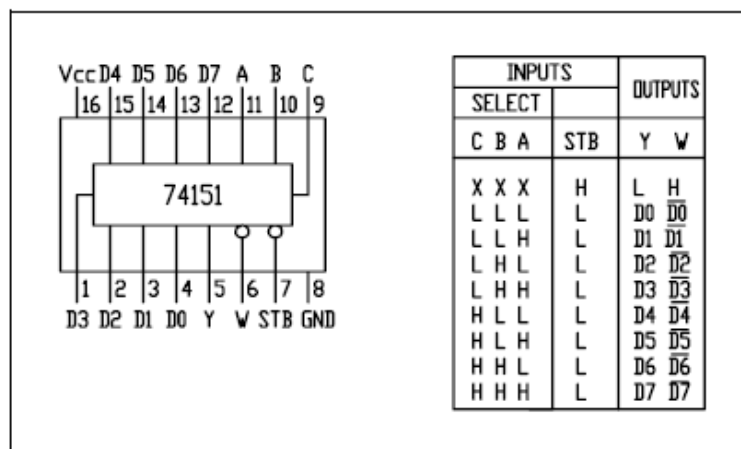

Figure 6.1 Connection Diagram and Truth Table of 74151

Almost any logic function can be implemented with data selectors. The simplest implementation is obtained when the function can be written either as a sum of products of logic variables. To implement a given function it is necessary to select a data selector which is able to satisfy all min-terms of the function, directly or through conditioning. The logic function of the 74151 is:

$F=A'B'C'D_0+A'B'CD_1+A'BC'D_2+A'BCD_3+AB'C'D_4+AB'CD_5+ABC'D_6+ABCD_7$

The logic function to be implemented can be obtained from the expression F by conditioning the desired min-terms and eliminating unused ones. A min-term is conditioned by applying the appropriate logic signal to its corresponding data input. Such a conditioning signal can vary from a simple logic 1 to the output signal of a complex gate array of combinational logic. Min-terms are eliminated by applying a logical 0 to the appropriate data inputs.

If more min-terms than available in the expression F are required, they may be created by appropriate conditioning of one or more data inputs and/or using more than one data selector.

ADDRESS DECODER / DEMULTIPLEXER

Address Decoders posses in general n address inputs and 2n outputs. Address inputs are decoded internally to validate one of the outputs in conjunction with control inputs. An example of built in address decoder is 74139. 74139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input (G1 or G2) can be used as a data input in demultiplexing applications. Figure 7.2 shows its connection diagram and truth table.
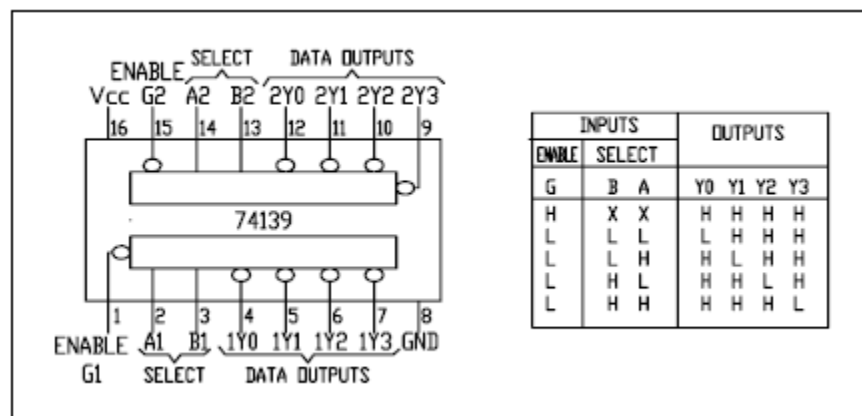

Figure 6.2 Connection Diagram and Truth Table of 74139

MEMORIES

A J-K flip-flop may be considered as a 1-bit memory unit. It is possible to build an n-bit memory using n J-K flip-flops with some decoders and data selectors. Figure 7.3 shows the block diagram of such a 4x1-bit RAM memory and its read-write cycles.

PREREQUISITE

- Implement Step 4 with Verilog on ISE.

EXPERIMENT

STEP1 By using the 74151 be familiar with its operation. For this purpose, connect the data-select and strobe inputs to level switches, the outputs to the indicator lamps. Apply any binary values to the data inputs.

STEP2 Implement the logic function f=A+B+C using a 74151 data selector.

STEP3 By using the 74139 be familiar with its operation.
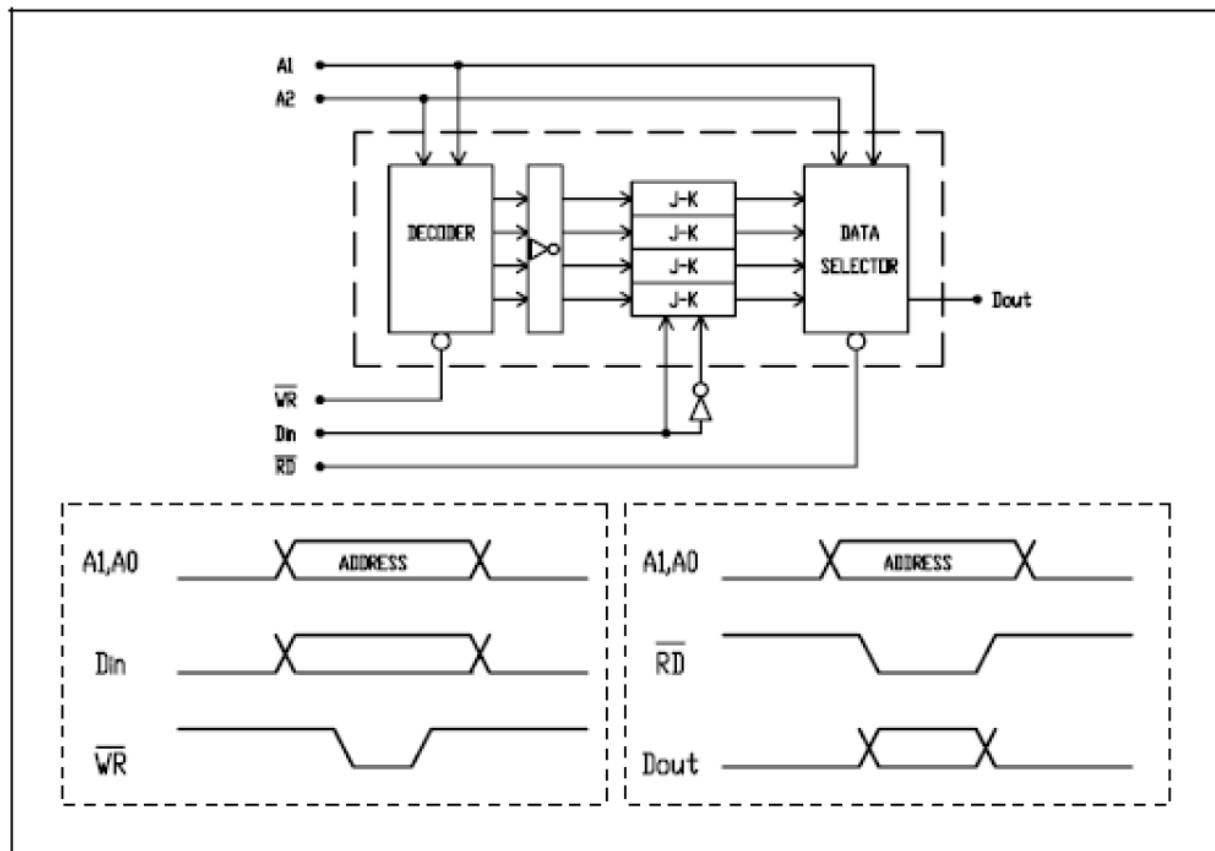
STEP4 Implement the 4x1-bit RAM of Figure 7.3.

Figure 6.3 An example 4x1-bit RAM Memory

COMPONENTS NEEDED

- A 7404 Hex Inverter
- Two 7476 Dual J-K Flip-flops
- A 74139 Address Decoder
- A 74151 Data Selector/Multiplexer

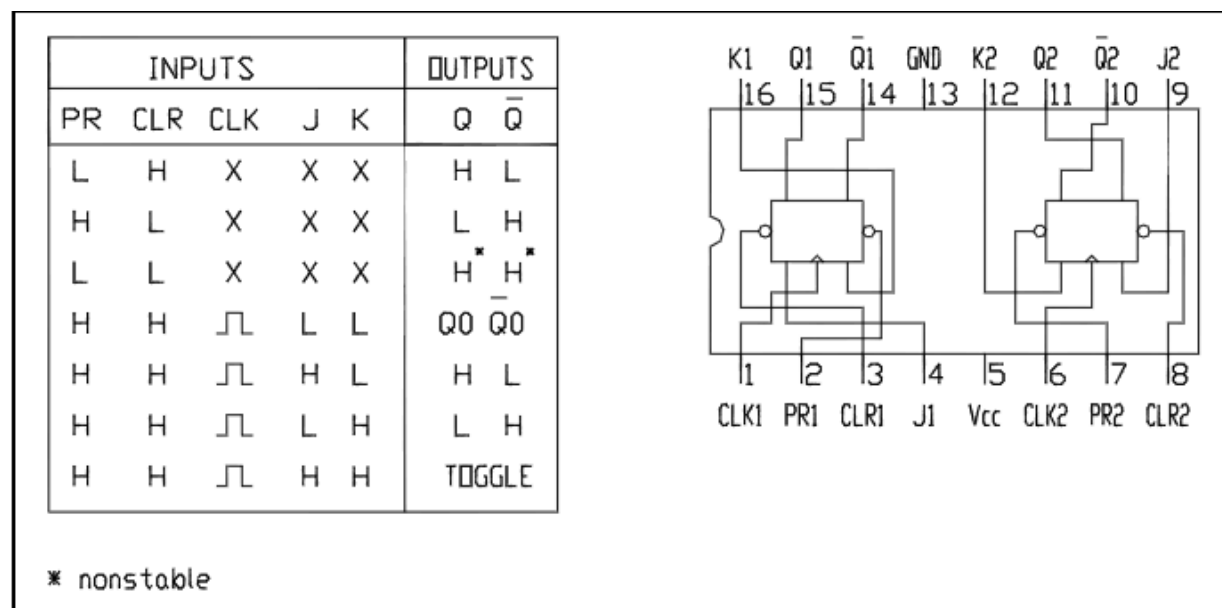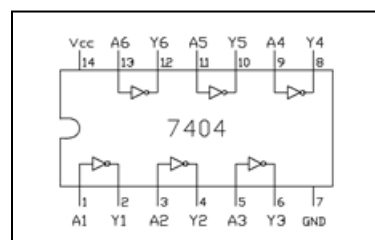| INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\overline{Q0}$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

* nonstable

Figure 6.4 JK Flip Flop

Figure 6.5 Hex Inverter