HACETTEPE UNIVERSITY

Department of Computer Science and Engineering

BBM233 Logic Design Laboratory

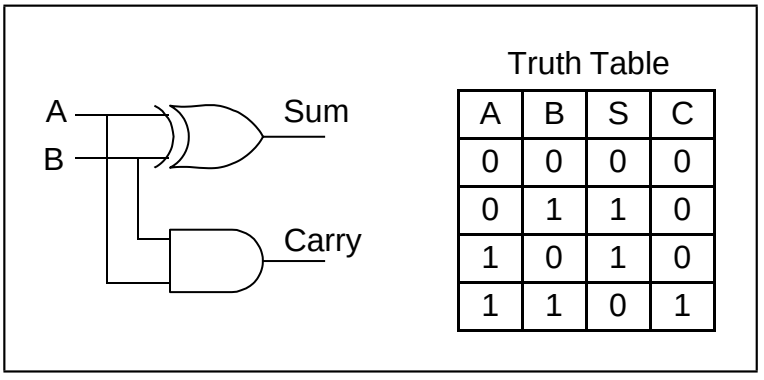
EXPERIMENT 2
ADDERS AND SUBTRACTERS

AIM

In this experiment circuits which perform arithmetic operations, namely half adder, full adder, half subtracter and full subtracter will be examined.

BACKGROUND

The basic arithmetic circuit is the adder. The simplest adder is called the half adder. The addition of an inverter to the half adder, converts it into a simple subtraction circuit called a half subtracter. An exclusive-OR (XOR) gate can be used as a conditional inverter that makes it possible to make the basic circuit a half adder or a half subtracter. The function of the circuit can be chosen by placing a logical 1 or a logical 0 on a mode input (one of the XOR inputs). Two half adder or subtracter circuits can be combined to form a full adder or subtracter.



Truth Table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

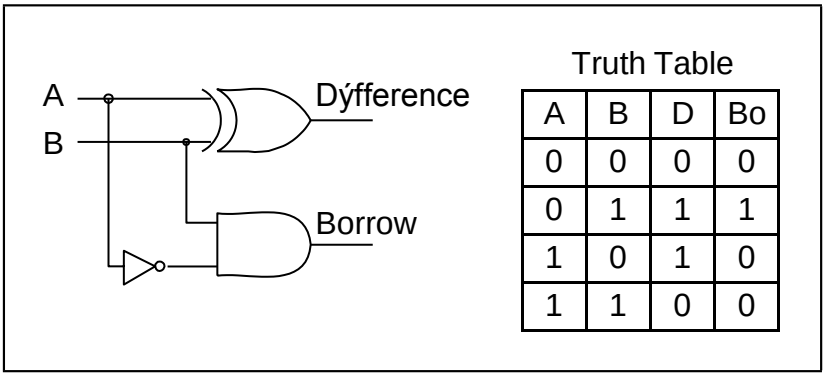
Figure 2.1. The Half Adder Circuit and its Truth Table

THE HALF ADDER

The half adder circuit adds two binary digits and forms a two digits sum. The least significant digit in the sum is labeled S (for sum); the most significant C (for carry). The circuit and the truth table of an half adder is shown in Figure 2.1. The summation equation is: $S = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$ and the carry equation is : $C = A \cdot B$

THE HALF SUBTRACTER

There are several ways of performing subtraction on a digital computer and these depend on how negative numbers are represented. The method described here is very similar to that for adding. When subtracting bits, it may be necessary to borrow from the higher order columns. The binary subtraction circuit and the truth table is shown in Figure 2.2. The difference (D) equation is: $S = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$ and the borrow (*Bo*) equation is $Bo = \overline{A} \cdot B$



A	B	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 2.2. The Half Subtracter Circuit and its Truth Table

THE CONDITIONAL INVERTER AND TRUE COMPLEMENT GENERATOR

An exclusive-OR gate can be made to invert a logic level or pass it on its true state. Figure 2.3 shows a combined half adder/subtracter circuits.

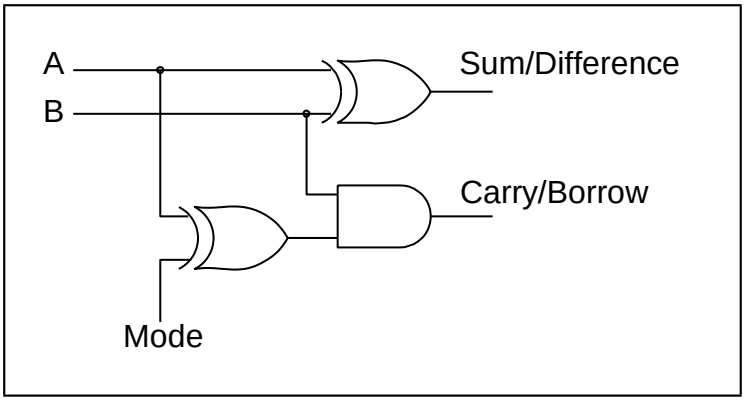


Figure 2.3. A Combined Half Adder/ Subtracter Circuit

THE FULL ADDER/SUBTRACTER

A circuit capable of adding two bits with carry is called a full adder. A full adder must have three inputs. A full subtracter perform subtraction between two bits with borrow when it is required. The full subtracter must also have three inputs. Two half adders/subtracters form a full adder/subtracter.

PREREQUISITE

- Implement Step 3 and Step 4 with Verilog on ISE.

EXPERIMENT

STEP1 Implement the circuit of Figure 2.1 and verify that it adds correctly.

STEP2 Connect the circuit shown in Figure 2.2 and verify that it subtracts correctly.

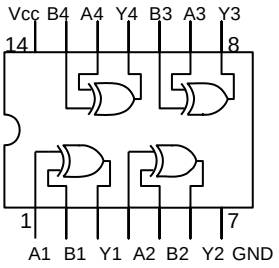
STEP3 Implement the circuit of Figure 2.3 and determine its truth table.

STEP4 Design and implement a full adder and determine its truth table.

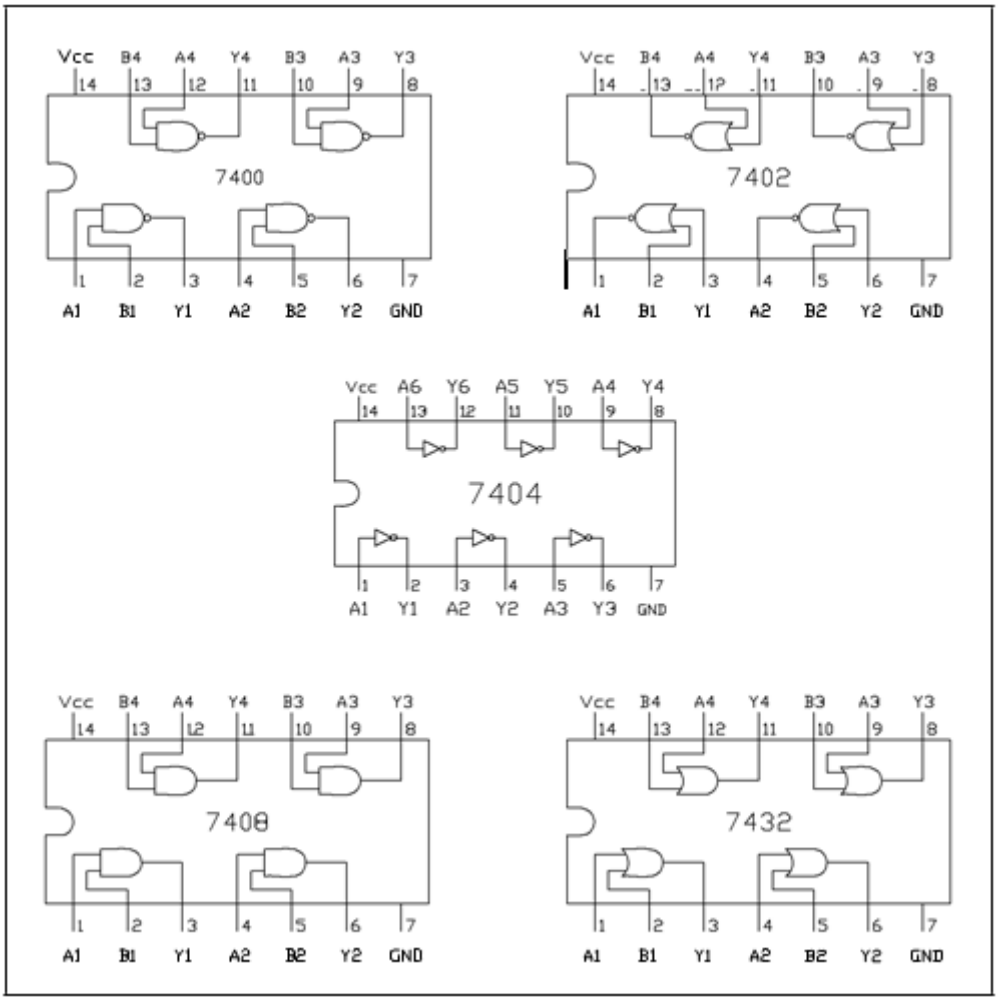
STEP5 Design and implement a full subtracter and determine its truth table.

COMPONENTS NEEDED

- A 7404 Hex Inverter
- A 7408 Quad 2-input AND Gate
- A 7432 Quad 2-input OR Gate
- A 7486 Quad 2-input XOR Gate



Connection diagram of 7486


Vcc B4 A4 Y4 B3 A3 Y3
14 13 12 11 10 9 8
7400
1 2 3 4 5 6 7
A1 B1 Y1 A2 B2 Y2 GND
Vcc B4 A4 Y4 B3 A3 Y3
14 13 12 11 10 9 8
7402
1 2 3 4 5 6 7
A1 B1 Y1 A2 B2 Y2 GND
Vcc A6 Y6 A5 Y5 A4 Y4
14 13 12 11 10 9 8
7404
1 2 3 4 5 6 7
A1 Y1 A2 Y2 A3 Y3 GND
Vcc B4 A4 Y4 B3 A3 Y3
14 13 12 11 10 9 8
7408
1 2 3 4 5 6 7
A1 B1 Y1 A2 B2 Y2 GND
Vcc B4 A4 Y4 B3 A3 Y3
14 13 12 11 10 9 8
7432
1 2 3 4 5 6 7
A1 B1 Y1 A2 B2 Y2 GND