HACETTEPE UNIVERSITY
Department of Computer Science and Engineering
BBM233 Logic Design Laboratory

EXPERIMENT 4
SHIFT REGISTERS

AIM

In this experiment shift registers will be examined.

BACKGROUND

A register is used to hold and manipulate a datum which is composed of a number of bits. Registers can in general be implemented using flip-flops. As it can be observed on the truth table given in Experiment 3, if J=0 and K=1, with the falling edge of the clock Q assumes state 0. Similarly, if J=1 and K=0, Q assumes state 1. The circuit of Figure 4.1 is known as a shift register and makes use of that property of the JK flip-flop. A shift register can be built up using a certain number of JK flip-flop. A shift register is used to rotate, if necessary bits stored in it.

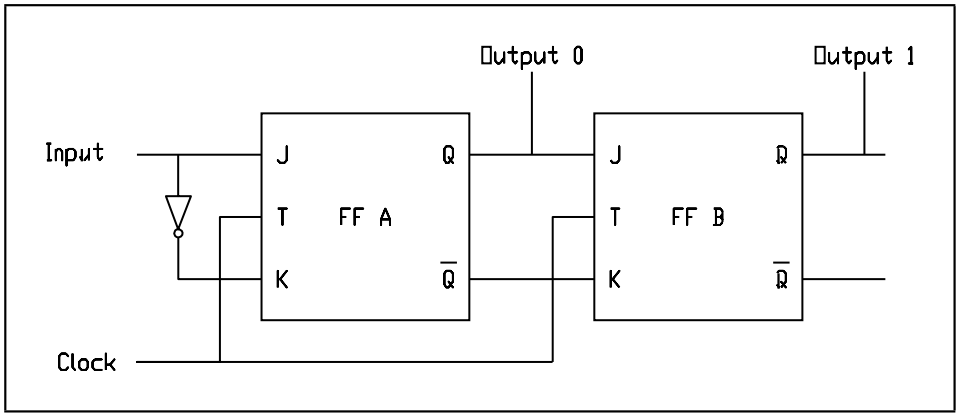

Figure 4.1 A two bit shift register

Shift registers are useful for making various types of counters, parallel to serial or serial to parallel converters, pseudo random sequence generators whereby delaying a sequence of binary digits by a prescribed number of clock pulses and for numerous of other applications.

A common form of marketed shift registers is a 4 bit parallel access shift register. Known under the serial number 7495, the 4 bit parallel access register features parallel and serial inputs, parallel outputs, mode control and two clock inputs. The register has three modes of operation:

1. Parallel Load

2. Shift Right (from output-A to output-D)
3. Shift Left (from output-D to output-A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flop and appears at the outputs after the high-to-low transition of the clock input. During loading, the entry of serial data is inhibited. Serial loading or shift operations are accomplished by taking the mode control input to low and producing clock pulses after applying data bits to the serial input. Figure 4.2 shows different modes of operations with 7495. A similar form in 8 bit format of 7495 is known under the serial number 74166.

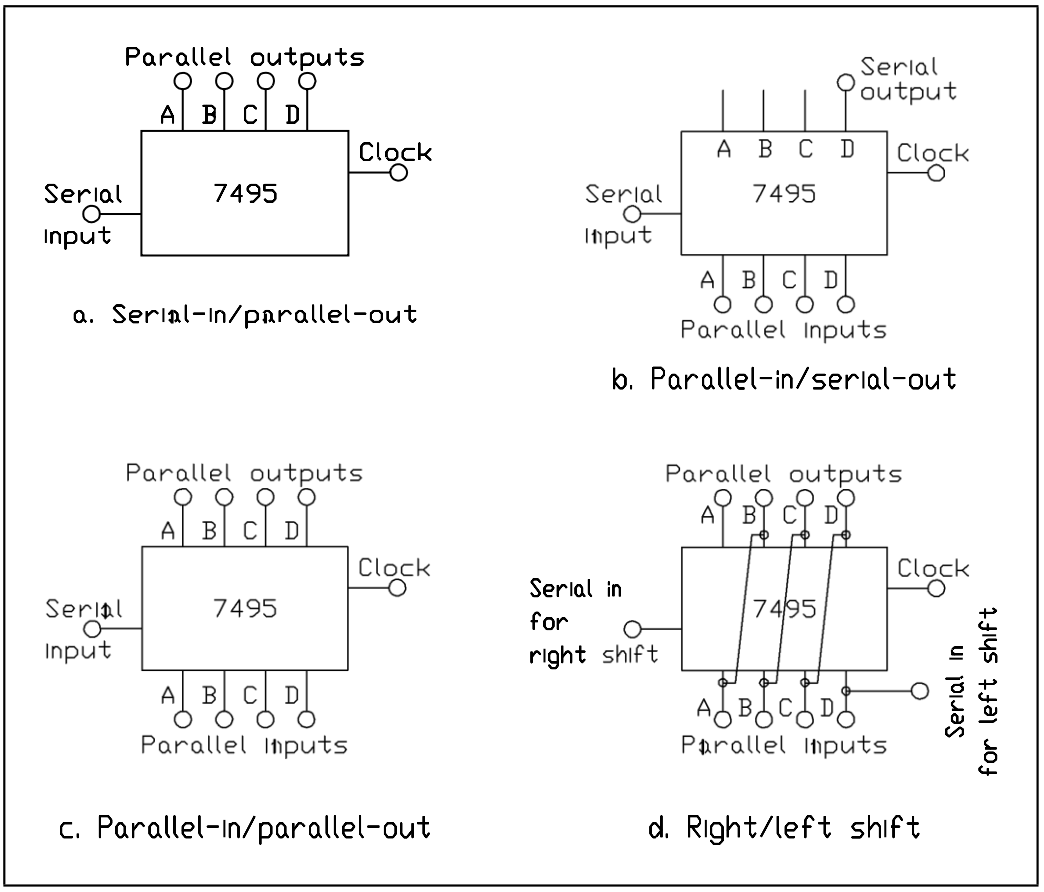

Figure 4.2 Modes of operations for 7495

PREREQUISITE

- Implement Step 1 with Verilog on ISE.

EXPERIMENT

STEP1 Implement the circuit (the 2 bit shift register) shown in Figure 4.1. Clear it to state 00. Once cleared load it to contain the binary 3 (with the least significant bit on the left) by controlling the input of the A flip-flop and the common clock. After this, set the input of the A flip-flop to 0 and shift the register once. What number does it contain now? Repeat the operation with 1 and 2 as initial contents of the register. Write down your observations with necessary explanations.

Remember that shifting a binary number to the right is equivalent to divide it by two and shifting to the left is equivalent to multiply it by two.

STEP2 Experiment with the serial-in/parallel-out mode of 7495.

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STEP5 Experiment with the serial-in/serial-out mode of 7495.

The operation *shift right* is accomplished on the falling edge (high-to-low transition) of clock-1 when mode control is low. Shift left is accomplished on the falling edge of clock-2 when the mode control is high. In the case of left shifting the output of each flip-flop should feed the input of the previous one such as output-D to input-C, output-C to input-B, etc. and the serial data should be applied to the input-D. The clock input may be applied simultaneously to clock-1 and clock-2 if both modes can be clocked from the same source. In this case there will be only one clock input as shown on Figure 4.2.

STEP6 Experiment with the shift left mode of 7495 (See Figure 4.2-d)

STEP7 Become familiar with 74166's operations. Use LEDs to display the states of the outputs.

COMPONENTS NEEDED

- 7404 Hex Inverter
- 7476 Dual JK Flip-flop
- 7495 4 bit-Parallel Access Shift Register
- 74166 8 bit-Parallel-in/Serial-out Shift Register

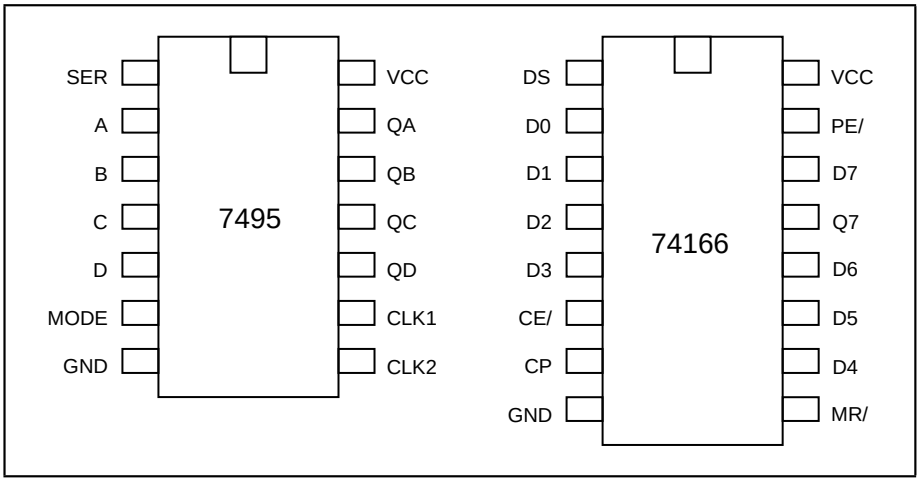

Figure 4.3 Pin configurations for 7495 and 74166.

PIN #	*SYMBOL*	*NAME AND FUNCTION*
1	DS	Serial data input
2,3,4,5,10,11,12,14	D0 to D7	Parallel data inputs
6	CE/	Clock enable input
7	CP	Clock input (L-to-H edge-trigged)
8	GND	Ground
9	MR/	Master reset input
13	Q7	Serial output from last stage
15	PE/	Parallel enable input
16	V_{CC}	Positive supply voltage (+5V)

Figure 4.4 Pin descriptions for 74166.

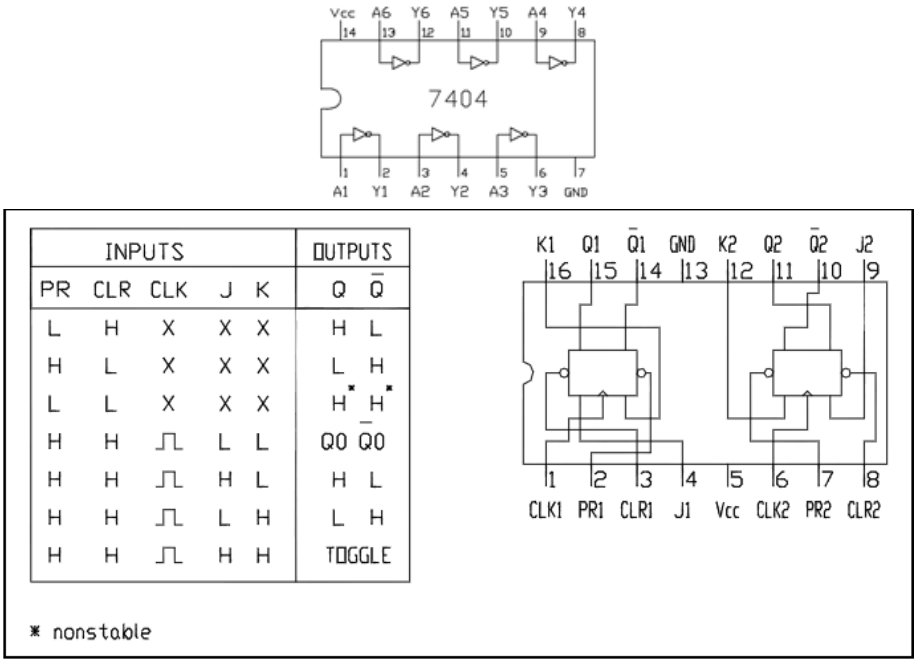

Figure 4.5 JK Flip Flop(7476) and Hex Inverter(7404).