HACETTEPE UNIVERSITY
Department of Computer Science and Engineering

BBM233 Logic Design Laboratory

EXPERIMENT 1
BASIC LOGIC GATES

AIM

In this experiment some basic logic gates such as AND, OR, NOT, NAND and NOR gates and some circuits resulting from their combinations will be examined.

BACKGROUND

The basic logic gates are:

1. the AND gate,
2. the OR gate and
3. the inverter (NOT gate).

As their names indicate these gates represent each a basic operation in Boolean Algebra. The AND and the OR gates can each have any number of inputs but only one output. The inverter has only one input and one output.

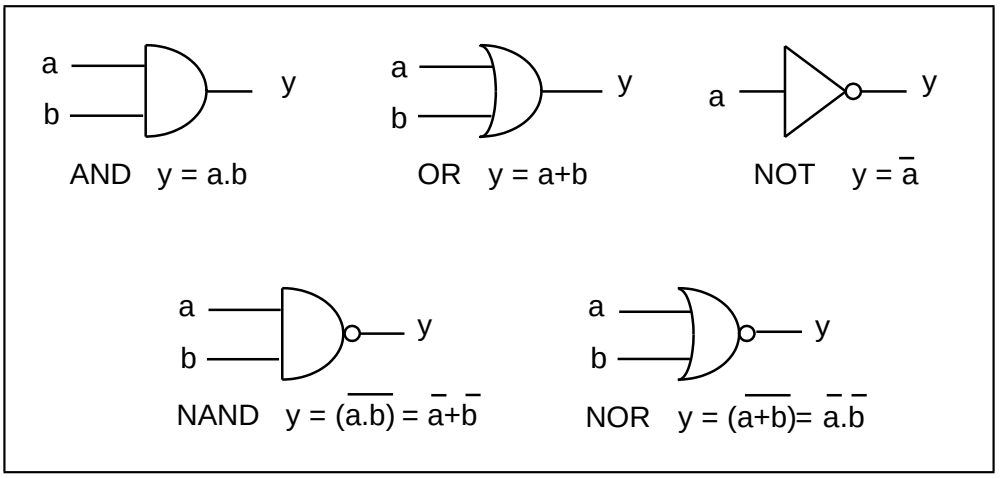

Figure 1.1. Symbols for Basic Logic Gates

The NAND gate is equivalent to the combination of an AND gate and an inverter (NOT gate). Therefore the word NAND is a contraction of the words NOT and AND. There is also NOR (NOT-OR) gate which is the concatenation of OR and NOT gates. Because the fabrication of NAND and NOR gates is much easier than the AND and OR's, these two combination gates represent the most popular off-the-shelf packages.

In the framework of digital electronic, logic gates give the possibility to perform Boolean Algebra operations on electrical signals. Within this context:

1. A logical 1 on the input or output of a gate corresponds to a relatively high voltage value designated as High, Hi or H.
2. A logical 0 on the input or output of a gate corresponds to a relatively low voltage value designated as Low, Lo, L.

As far as the TTL[1] technology of IC fabrication is concerned:

- a low level is defined as any voltage between 0 and 0.8 volt,
- a high level is defined as any voltage between 2.0 to 5 V.

PREREQUISITE

- Implement Step 6 with Verilog on ISE.

EXPERIMENT

1. Verify the truth table for a 2-input AND gate.
2. Verify the truth table for a 2-input OR gate.
3. Verify the truth table for a 2-input NAND gate.
4. Verify the truth table for a 2-input NOR gate.
5. Verify the truth table for a NOT gate.
6. Implement the Boolean function
   $y=a \oplus b \oplus c$ where $\oplus$ represents the *exclusive OR* operation.

Please follow carefully the procedure given below while implementing your circuits during the experiments.

- Be sure first that the power switch is off.
- Start by preparing input and output modules such as switches before proceeding to the cabling of the circuit itself.
- Connect GND to ground and Vcc to + 5V on the board.
- Check the connections, don't forget to connect V_{cc} and GRD on the ICs, then turn the power on.
- Turn the power off once you have finished with the experiment.

[1] Transistor-Transistor-Logic. A complete taxinomy of IC fabrication technologies should take place in your experiment report.

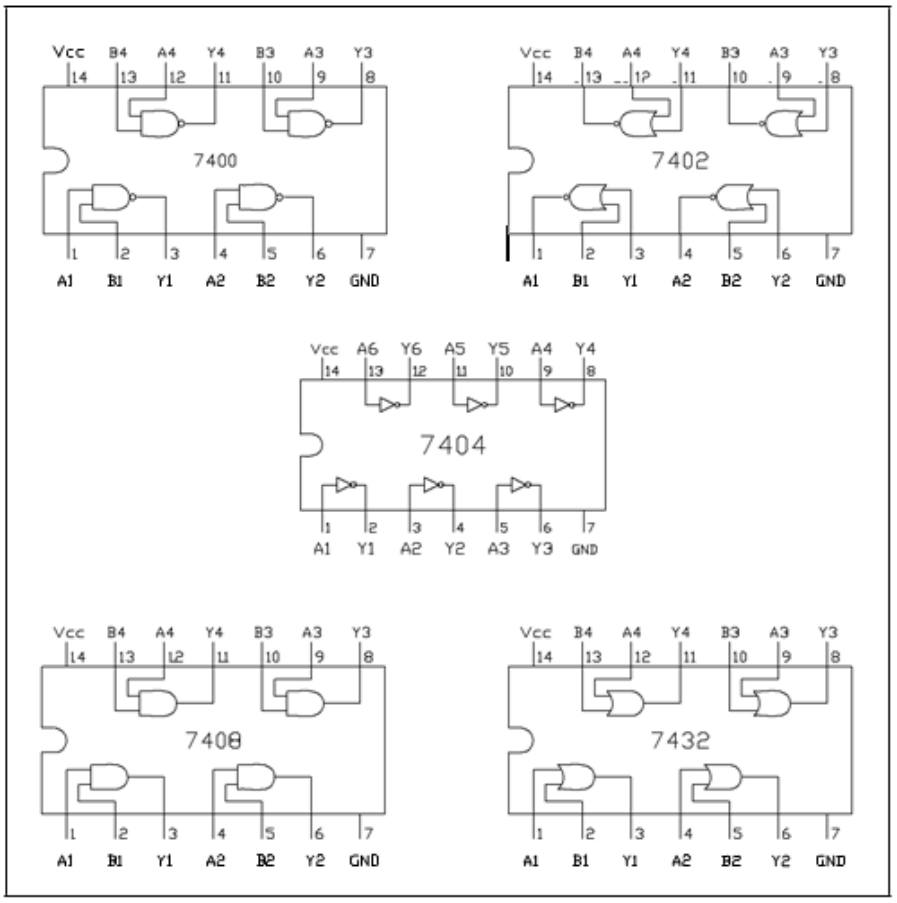

Figure 1.3. The connection diagram for some ICs.

COMPONENTS NEEDED

- 1 x 7400 Quad 2-input NAND Gate
- 1 x 7402 Quad 2-input NOR Gate
- 1 x 7404 Hex Inverter
- 1 x 7408 Quad 2-input AND Gate
- 1 x 7432 Quad 2-input Or Gate