HACETTEPE UNIVERSITY
Department of Computer Science and Engineering
BBM233 Logic Design Laboratory

EXPERIMENT5
COUNTERS

AIM

In this experiment different type of counters such as binary ripple up/down, divide by n, Johnson, synchronous counters and their principle and internal structure will be examined.

BACKGROUND

Counters are sequential circuits that return to their initial state after a specified number of changes in the input state. Counters are being used extensively in industrial and laboratory environments for such functions as controlling the position of a machine tool, packing a specified number of items in a box, counting frequency, recording time, speed and acceleration etc. There are numerous types of counters and several ways of implementing each type.

THE BINARY RIPPLE UP COUNTER

The Binary Ripple Up counter is the most basic and simplest of binary counters. It counts from 0 to $2^{(n-1)}$. The internal structure of such counter is given in Figure 5.1.

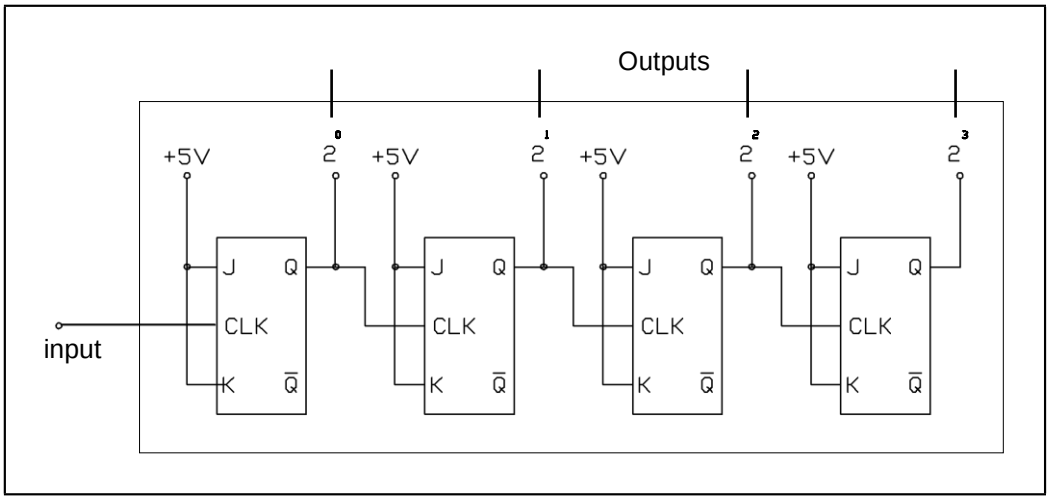

Figure 5.1 Binary Ripple up counter

THE BINARY RIPPLE DOWN COUNTER

The Binary Ripple Down Counter is similar to the Binary Ripple Up counter. Instead of counting upwards it is designed to count downwards from $2^{(n-1)}$ to 0.

THE DIVIDE-BY-N COUNTER

These counters are also called Mod N counters and count from 0 to N-1. For instance a divide-by-3 counter counts from 0 to 2 and its counting sequence is 0,1,2,0,1,2,...The internal structure of a divide-by-3 counter is shown in Figure 5.2.

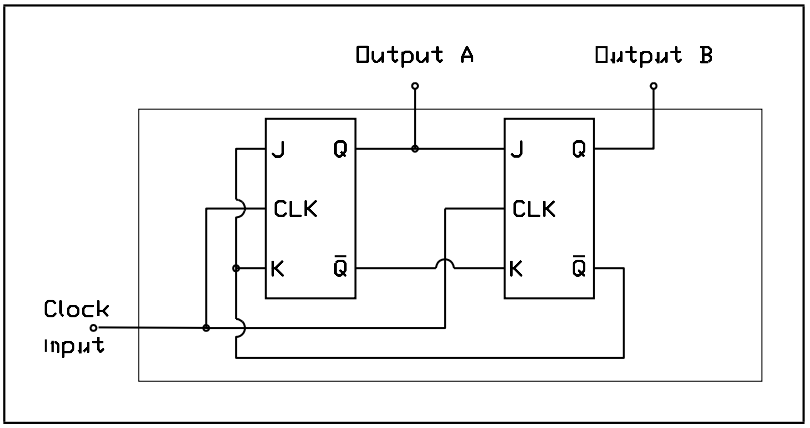

Figure 5.2 Divide-by-3 counter

THE JOHNSON COUNTER

The Johnson codes for two, three, and four digits are listed below. Counters using this code are called Johnson or twisted ring counters. Remember that Johnson code is a non-weighted code. Johnson counters can be implemented using shift registers. Figure 5.3 shows a sample circuit.

Johnson Codes

	ab	abc	abcd
0	00	000	0000
1	10	100	1000
2	11	110	1100
3	01	111	1110
4		011	1111
5		001	0111
6			0011
7			0001

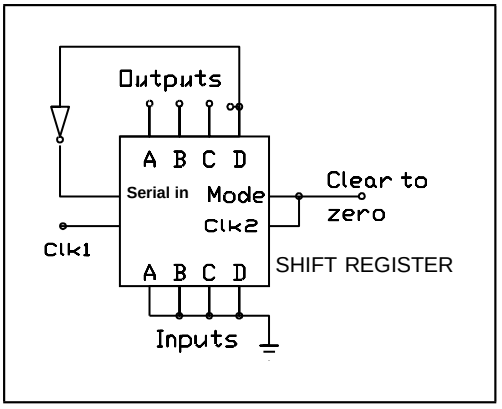

Figure 5.3 Johnson counter

PREREQUISITE

- Implement Step 1 and Step 3 with Verilog on ISE.

EXPERIMENT

STEP1 Implement the circuit of Figure 5.1 and become familiar with its operation.

STEP2 Implement the circuit of Figure 5.2 and become familiar with its operation.

STEP3 Design and implement a Divide-by-5 counter using flip-flops and some additional logic gates.

STEP4 Implement the circuit of Figure 5.3. Become familiar with its operation,

STEP5 With the circuit of Figure 5.3, instead of clearing the register to zero, load one of the disallowed input combinations and start counting from that combination. Proceed till you come back to the same state. Try three illegal starting states and write down your observations.

COMPONENTS NEEDED

- A 7404 Hex Inverter
- A 7408 Quad 2-input AND Gate
- A 7432 Quad 2-input OR Gate
- Two 7476 Dual JK Flip-flop
- A 7495 4-bit Parallel Access Shift Register

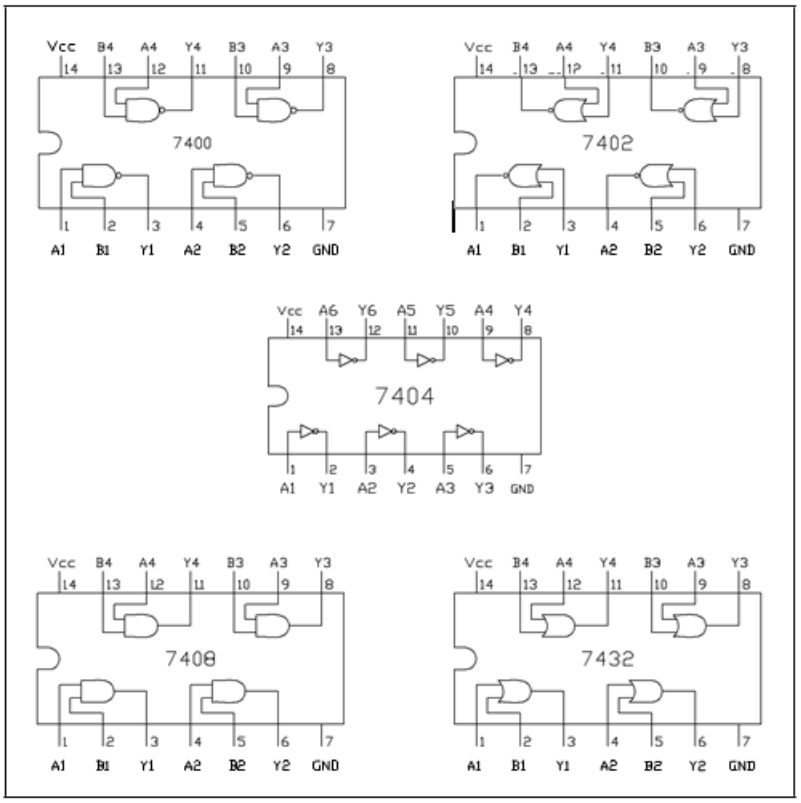

Figure 5.4 Basic Logic Gates

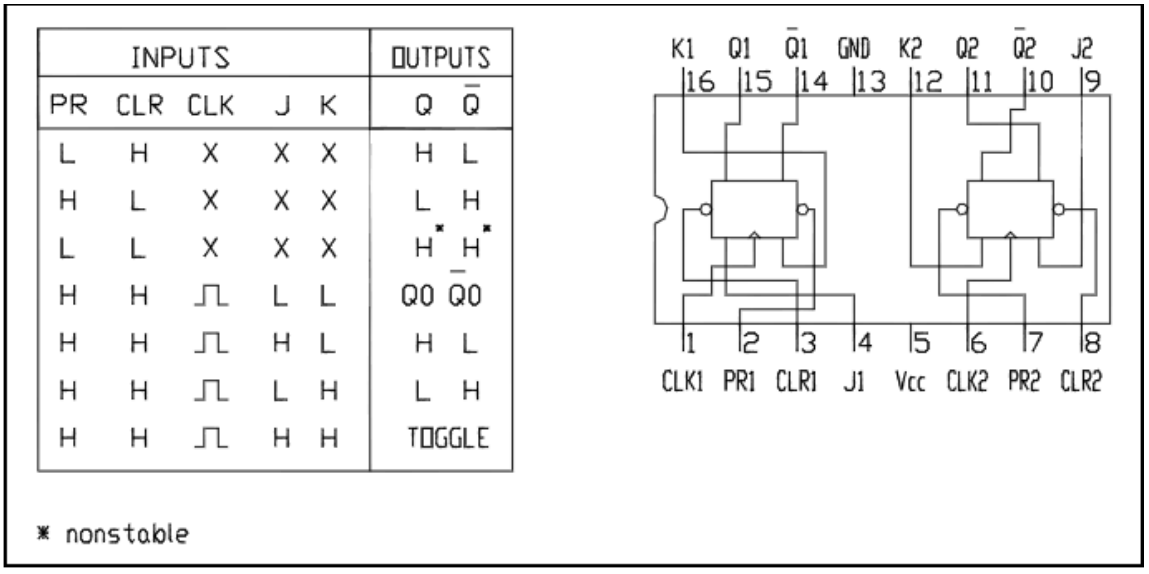

Figure 5.5 J-K Flip-flops

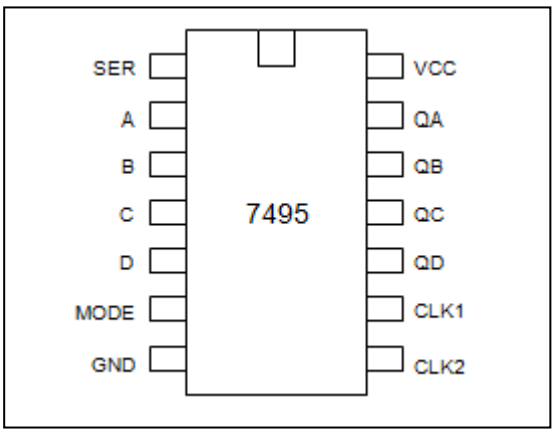

Figure 5.6 7495 Shift Register