Midterm Review

Logic Design – BBM231

Q1

Design a four-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer?

Q1

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1's complement: flip
2's complement: flip + 1

Q1

Design a four-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer?

a) truth table

Q1

Design a four-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer?

a) truth table
b) K-map
c) solve K-map

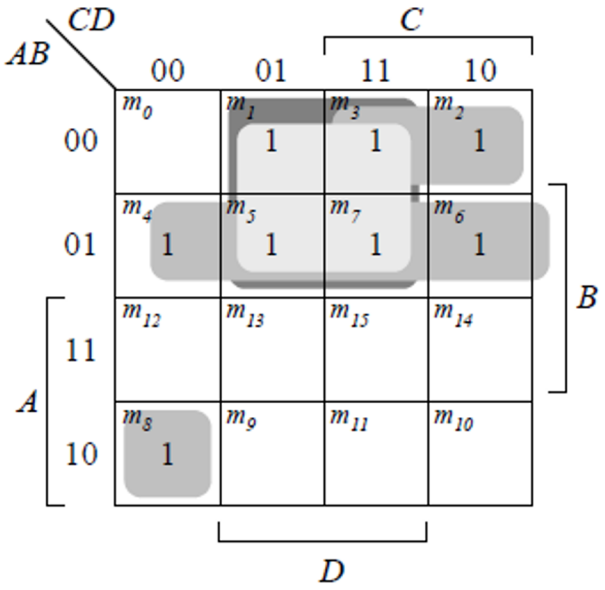
Q1

ABCD	wxyz
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

Q1

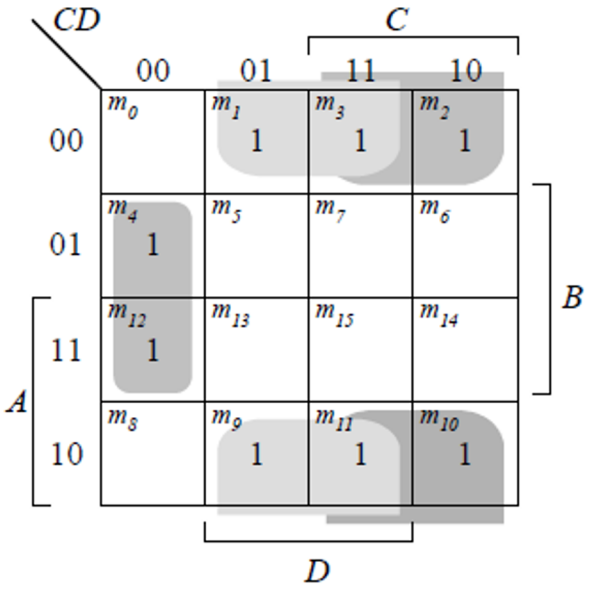
ABCD	wxyz
0000	0000
0001	1111
0010	1110
0011	1101
0100	1100
0101	1011
0110	10 10
0111	100 1
1000	1000
1001	0111
1010	0110
1011	0101
1100	0100
1101	0011
1110	0010
1111	0001

Q1


CD
AB
C
00
01
11
10
m_0 m_1 m_3 m_2
m_4 m_5 m_7 m_6
m_{12} m_{13} m_{15} m_{14}
m_8 m_9 m_{11} m_{10}
1
B
A
D

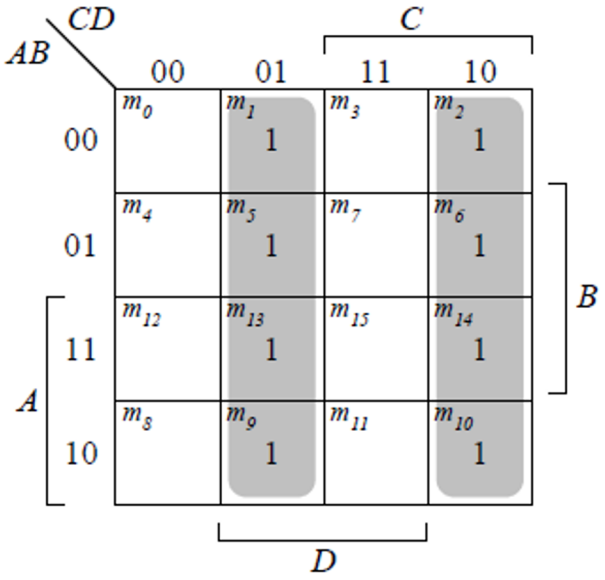
$w =$

$=$

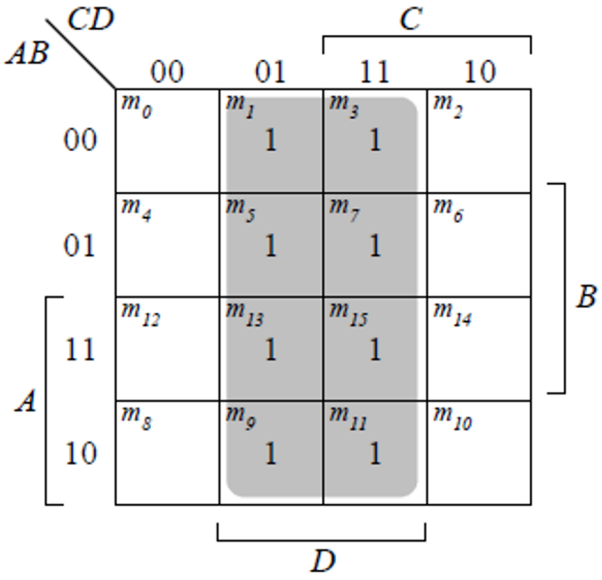

CD
C
00
01
11
10
m_0 m_1 m_3 m_2
m_4 m_5 m_7 m_6
m_{12} m_{13} m_{15} m_{14}
m_8 m_9 m_{11} m_{10}
1
B
A
D

$x =$

$=$

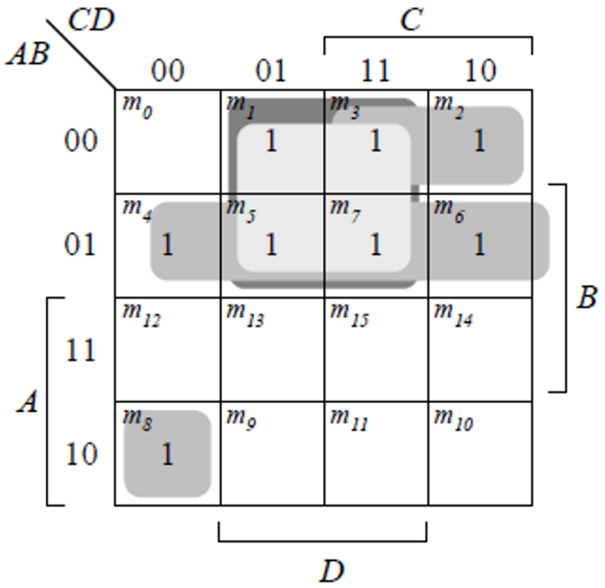

CD
AB
C
00
01
11
10
m_0 m_1 m_3 m_2
m_4 m_5 m_7 m_6
m_{12} m_{13} m_{15} m_{14}
m_8 m_9 m_{11} m_{10}
1
B
A
D

$y =$


CD
AB
C
00
01
11
10
m_0 m_1 m_3 m_2
m_4 m_5 m_7 m_6
m_{12} m_{13} m_{15} m_{14}
m_8 m_9 m_{11} m_{10}
1
B
A
D

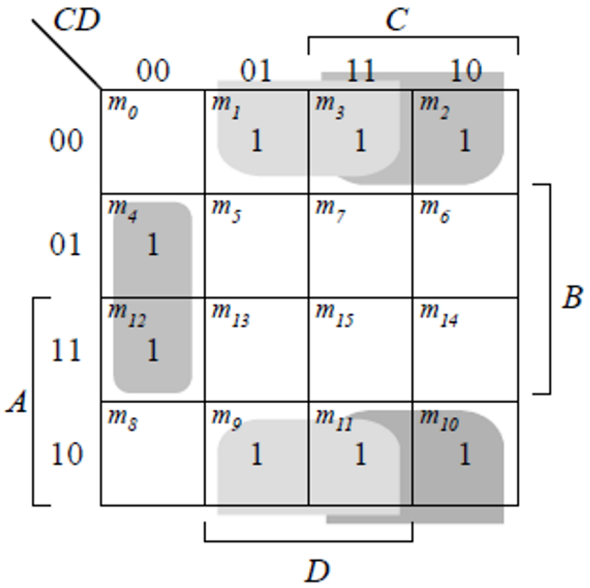
$z =$

Q1



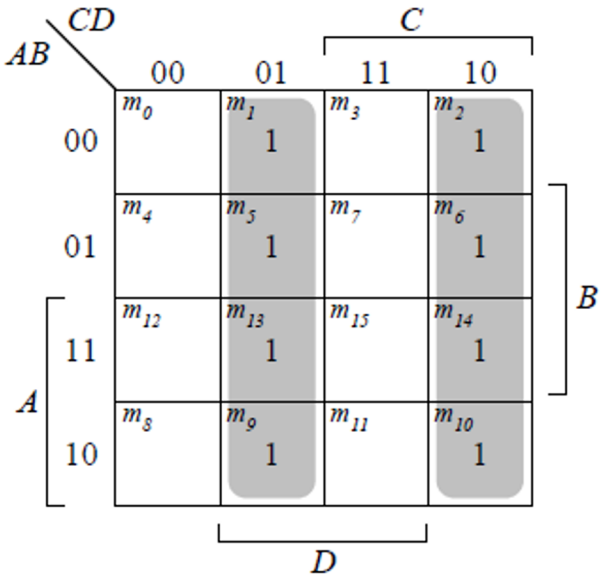
$w = A'(B + C + D) + AB'C'D'$

$= A \oplus (B + C + D)$

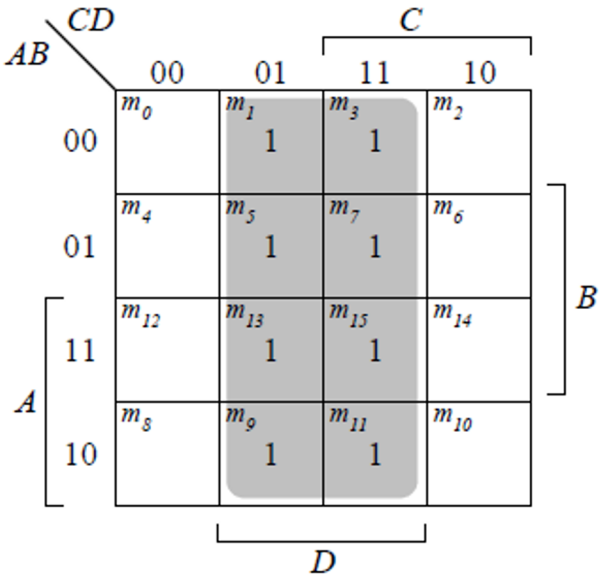


$x = B'(C + D) + CB'D'$

$= B \oplus (C + D)$



$y = CD' + C'D = C \oplus D$



$z = D$

Q1

For a 5-bit 2's complementer with input E and output v:

$$v = E \oplus (A + B + C + D)$$

Q2

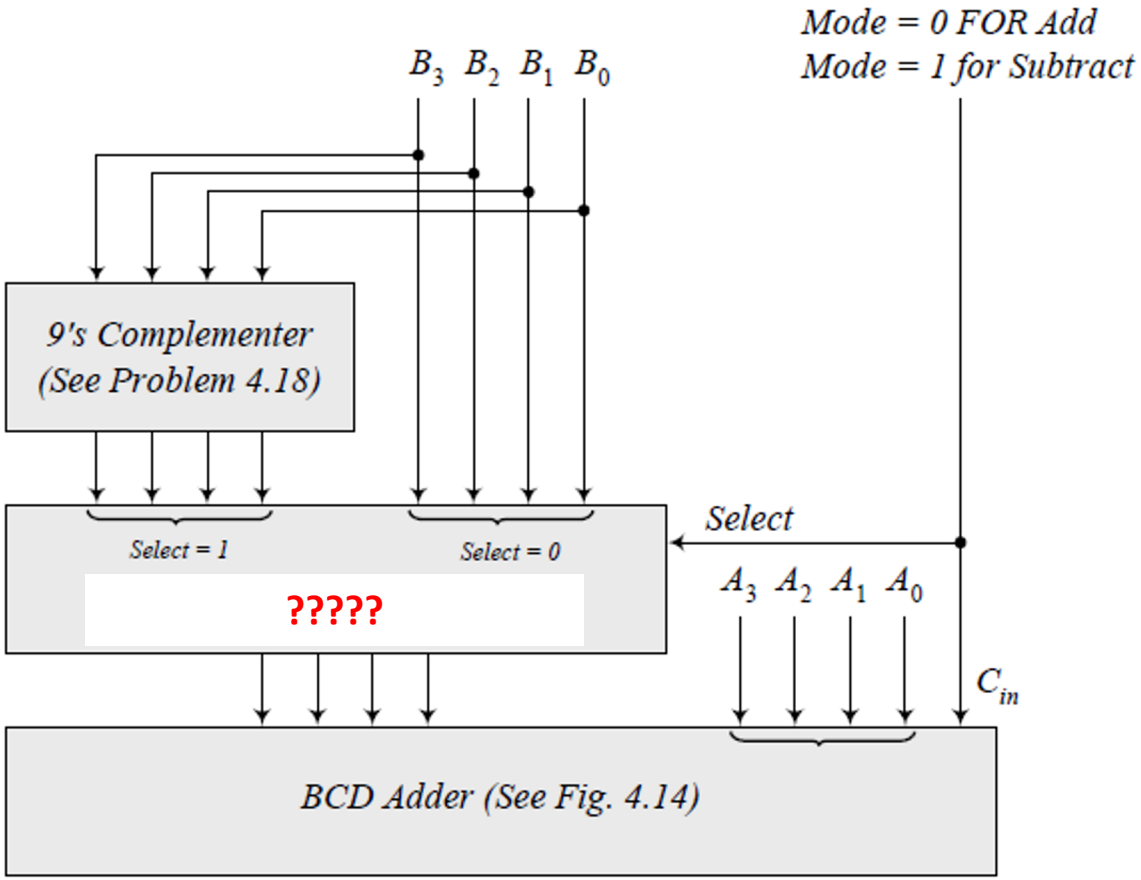
Construct a 4-bit BCD adder–subtractor circuit. Use the BCD adder and the 9's complementer. Use block diagrams for the components.

9’s complement subtraction

	Regular Subtraction	9's Complement Subtraction	
(a)	8	8	
	− 2	+ 7	9's complement of 2
	6	(1) 5	
		+ 1	Add carry to result
		6	
(b)	28	28	
	− 13	+ 86	9' complement of 13
	15	(1) 14	
		+ 1	Add carry to the result
		15	
(c)	18	18	
	− 24	+ 75	9' complement of 24
	−6	93	9's complement of result (No carry indicates that the answer is negative and in complement form)
		−06	

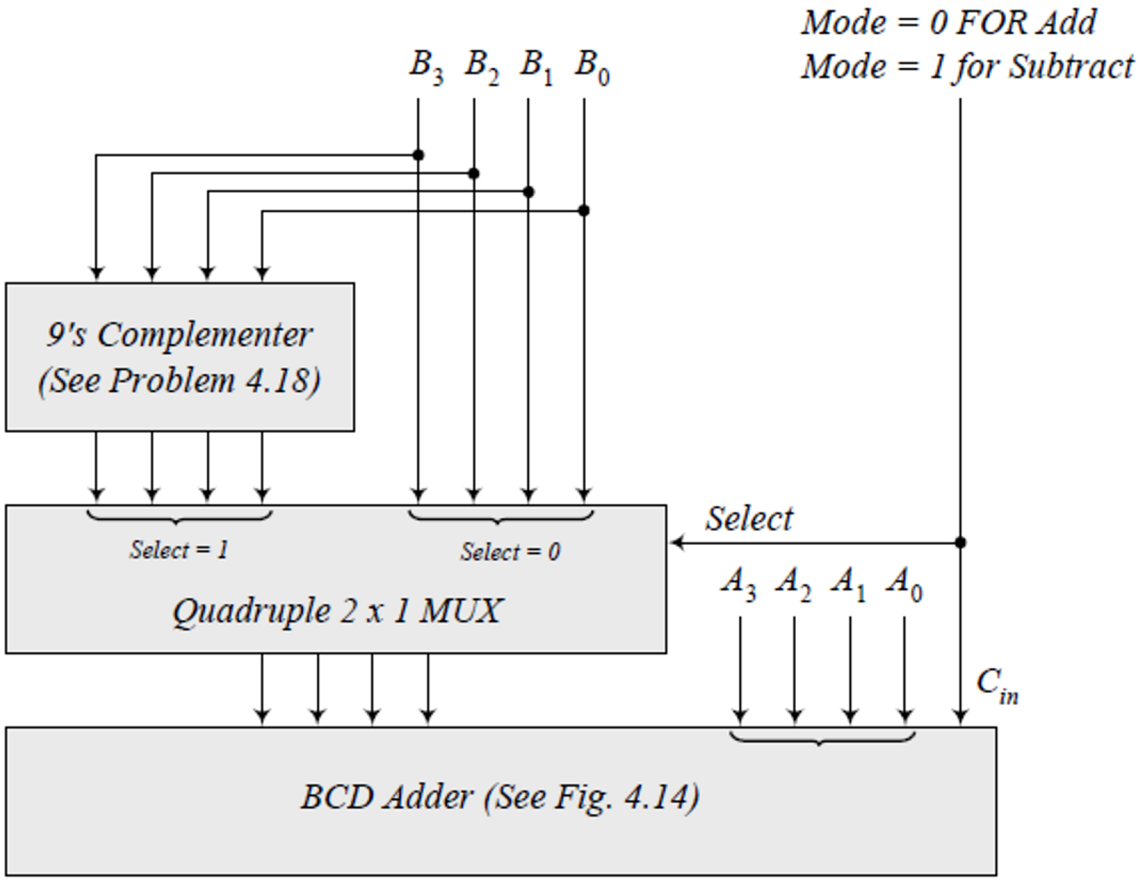
Q2

Construct a 4-bit BCD adder–subtractor circuit. Use the BCD adder and the 9's complementer. Use block diagrams for the components.



Q2

Construct a 4-bit BCD adder–subtractor circuit. Use the BCD adder and the 9's complementer. Use block diagrams for the components.



Q3

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

Q3

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

Do we know a logic gate that outputs 1 only if its both inputs are the same?

Q3

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

Remember XOR is the Odd Function?
What is an Odd Function?

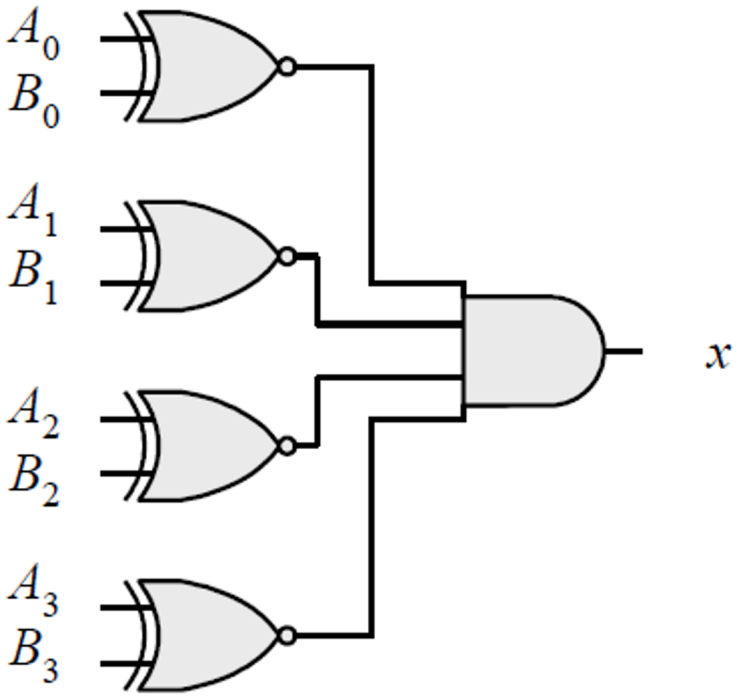
Q3

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

Then how about **XNOR**?

Q3

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

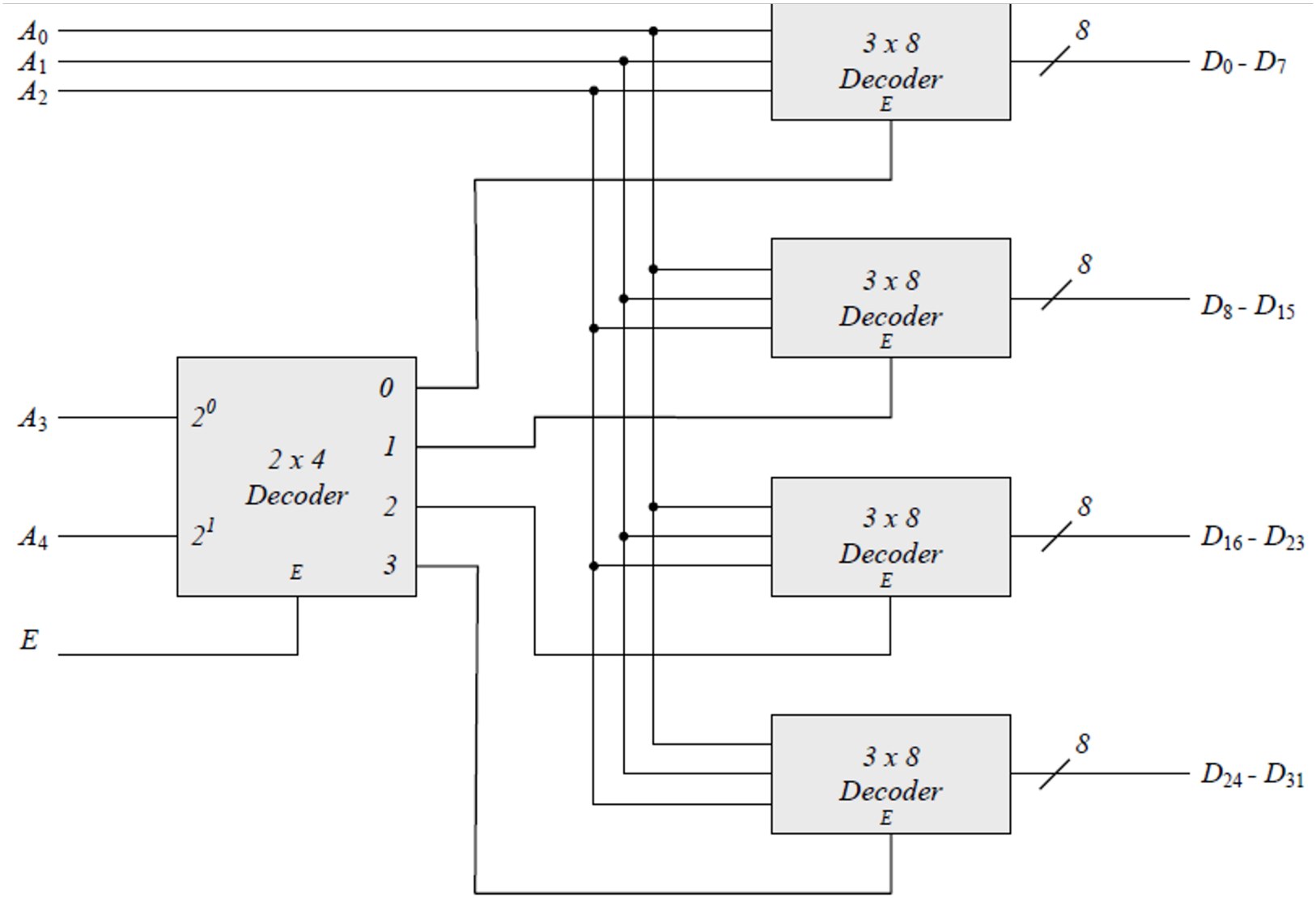


$$x = (A_0 \oplus B_0)'(A_1 \oplus B_1)'(A_2 \oplus B_2)'(A_3 \oplus B_3)'$$

Q4

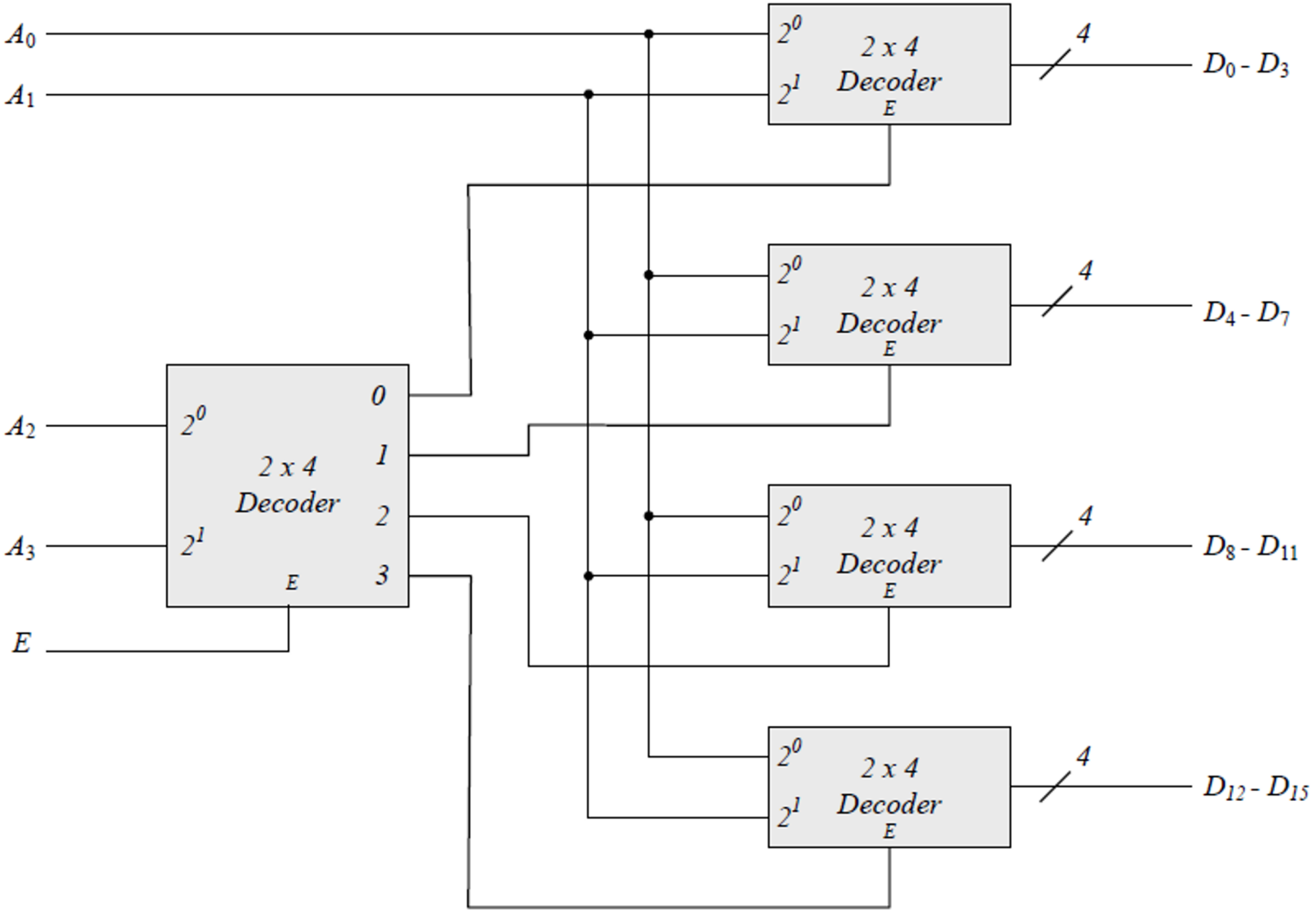
Construct a 5-to-32-line decoder with enable using four 3-to-8-line decoders with enable and a 2-to-4-line decoder with enable. Use block diagrams for the components.

Q4 Construct a 5-to-32-line decoder with enable using four 3-to-8-line decoders with enable and a 2-to-4-line decoder with enable. Use block diagrams for the components.



Q5 Construct a 4-to-16-line decoder with enable using five 2-to-4-line decoders with enable.

Q5 Construct a 4-to-16-line decoder with enable using five 2-to-4-line decoders with enable.



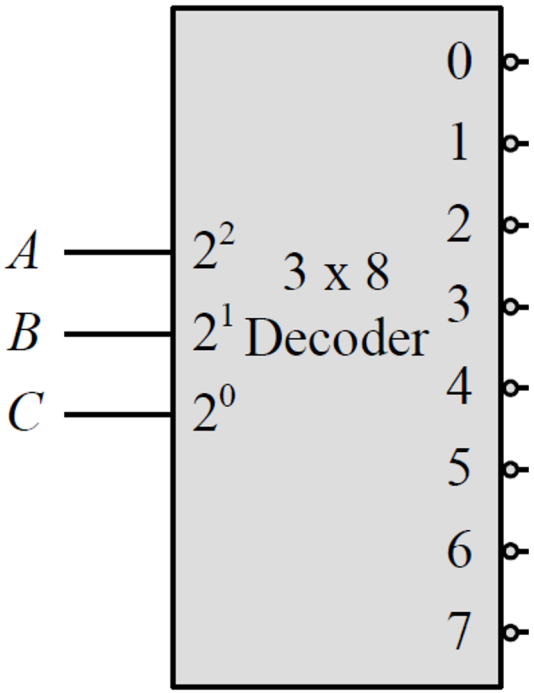
Q6

A combinational circuit is specified by the following three Boolean functions:

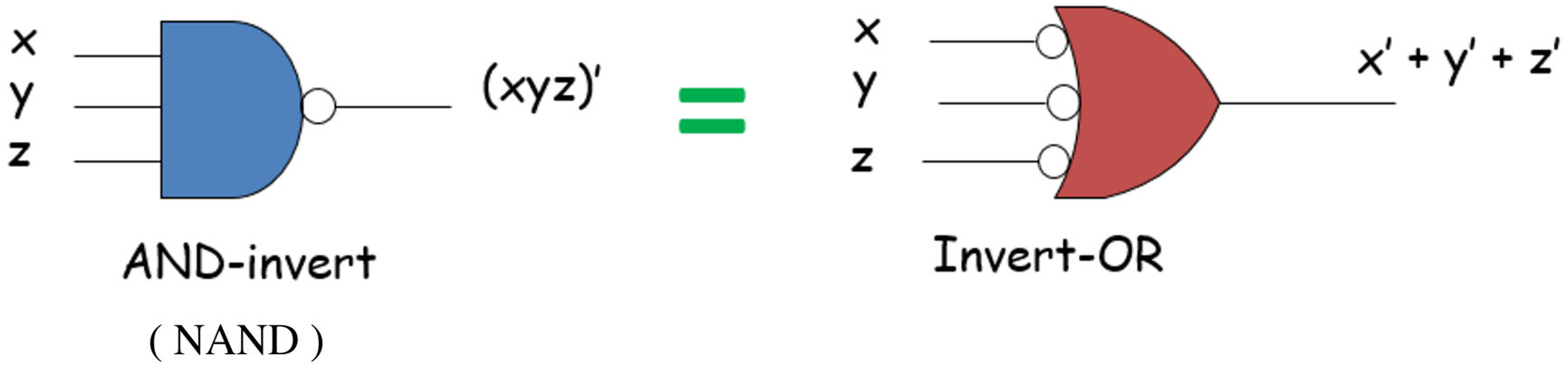
$$F_1(A, B, C) = \Sigma(1, 4, 6)$$
$$F_2(A, B, C) = \Sigma(3, 5)$$
$$F_3(A, B, C) = \Sigma(2, 4, 6, 7)$$

Implement the circuit with a decoder and NAND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

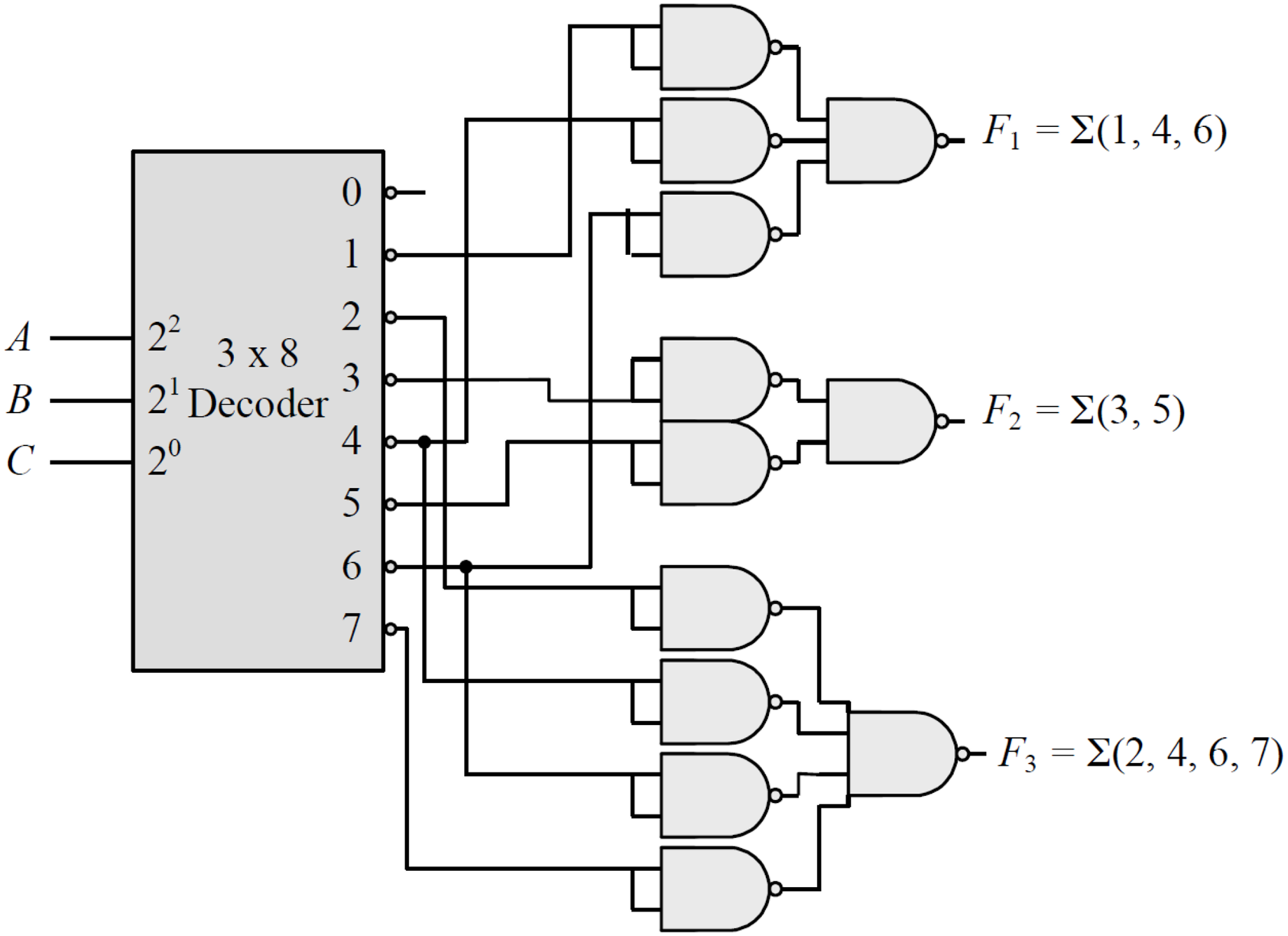
Q6



Q6



Q6


A
B
C
2^2
2^1
2^0
3 x 8
Decoder
0
1
2
3
4
5
6
7
$F_1 = \Sigma(1, 4, 6)$
$F_2 = \Sigma(3, 5)$
$F_3 = \Sigma(2, 4, 6, 7)$

Q7

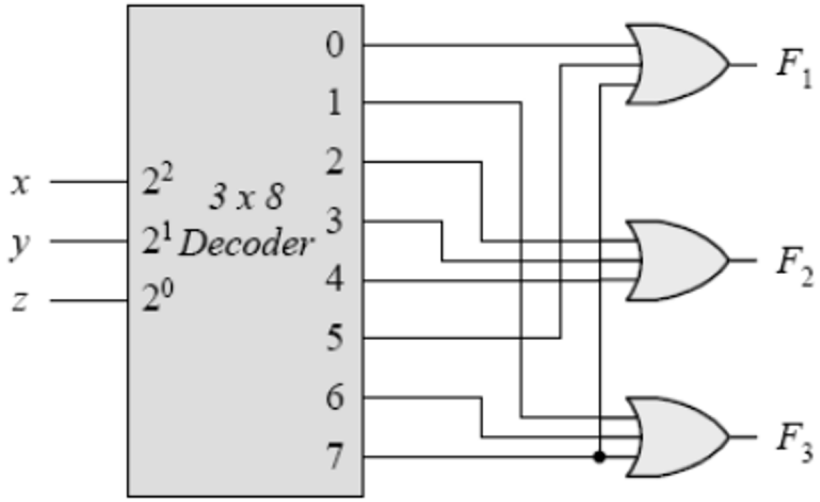
$$F_1 = x'yz' + xz$$
$$F_2 = xy'z' + x'y$$
$$F_3 = x'y'z' + xy$$

Implement the functions with one decoder and OR gates

Q7

$$F_1 = x'yz' + xz$$
$$F_2 = xy'z' + x'y$$
$$F_3 = x'y'z' + xy$$

$$F_1 = x(y + y')z + x'yz' = xyx + xy'z + x'yz' = \Sigma(2, 5, 7)$$
$$F_2 = xy'z' + x'y = xy'z' + x'yz + x'yz' = \Sigma(2, 3, 4)$$
$$F_3 = x'y'z' + xy(z + z') = x'y'z' + xyz + xyz' = \Sigma(0, 6, 7)$$



Q9

Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.

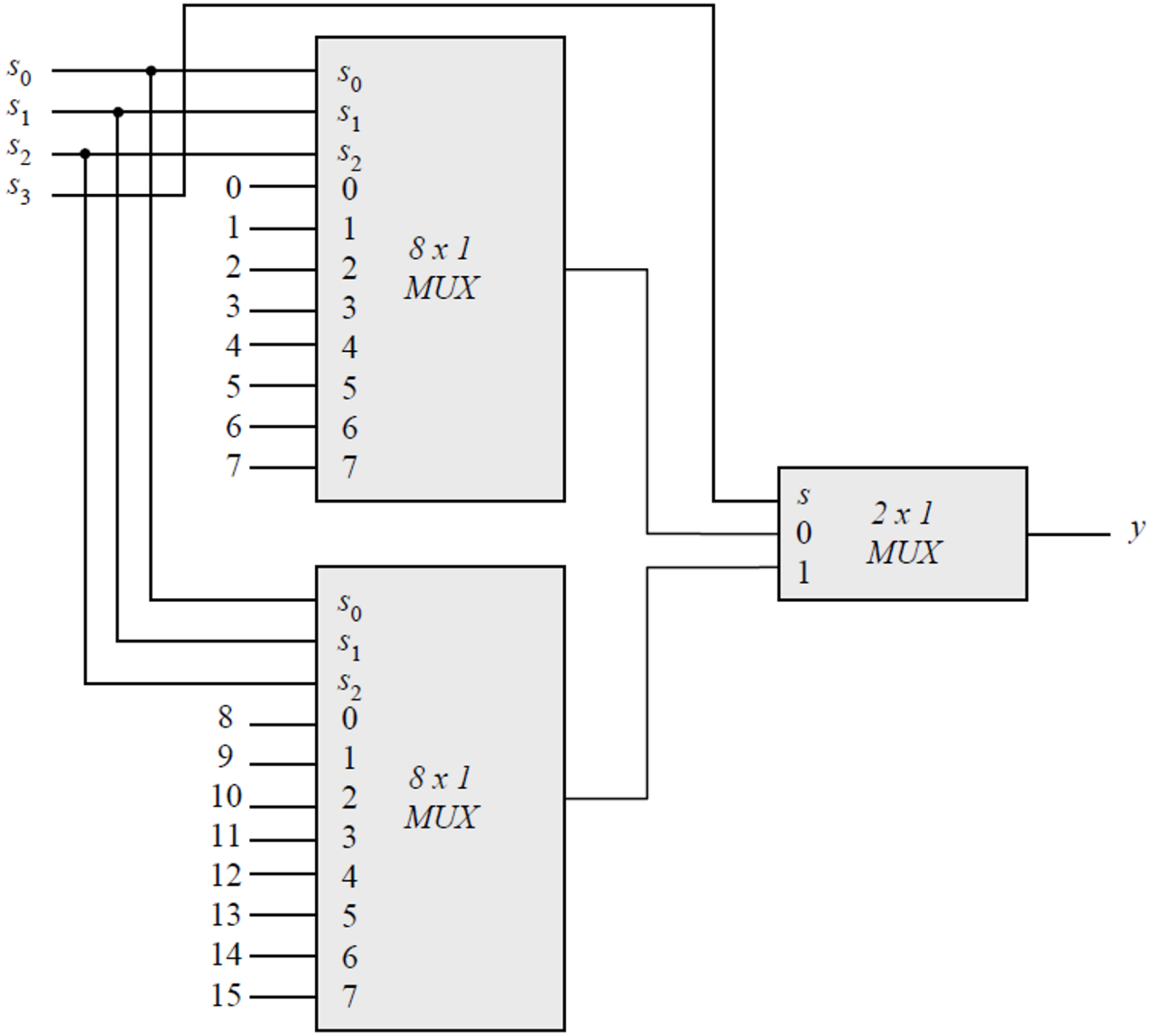
Q9

Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.

a) How many inputs?
b) How many selection lines?

Q9

Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.



Q10

Implement the following Boolean function with a multiplexer

(a) $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

Q10

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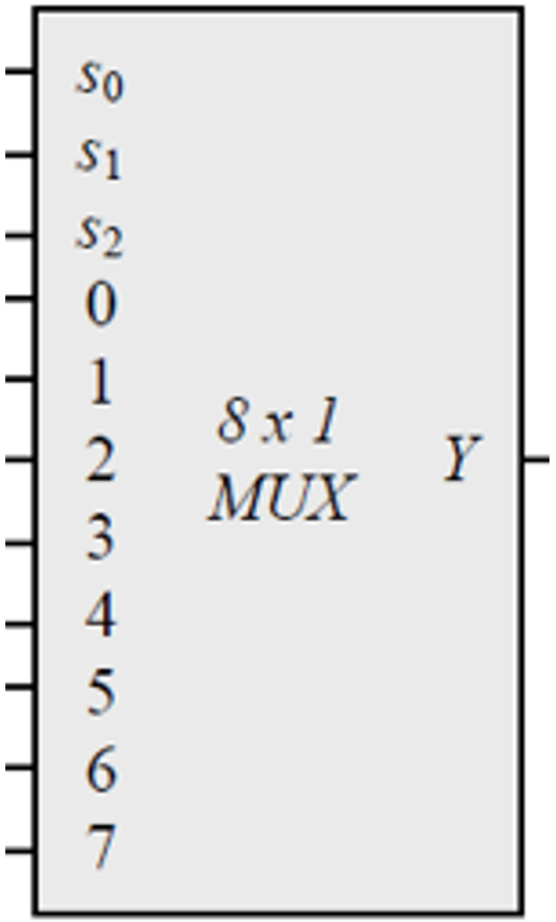


Q10

Implement the following Boolean function with a multiplexer

(a) $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

Inputs *ABCD*
000 0
000 1
001 0
001 1
010 0
010 1
011 0
011 1
100 0
100 1
101 0
101 1
110 0
110 1
111 0
111 1

Q10 $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

Inputs ABCD	*Mux input line (ABC)*
000 0	0
000 1	0
001 0	1
001 1	1
010 0	2
010 1	2
011 0	3
011 1	3
100 0	4
100 1	4
101 0	5
101 1	5
110 0	6
110 1	6
111 0	7
111 1	7

Q10 $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

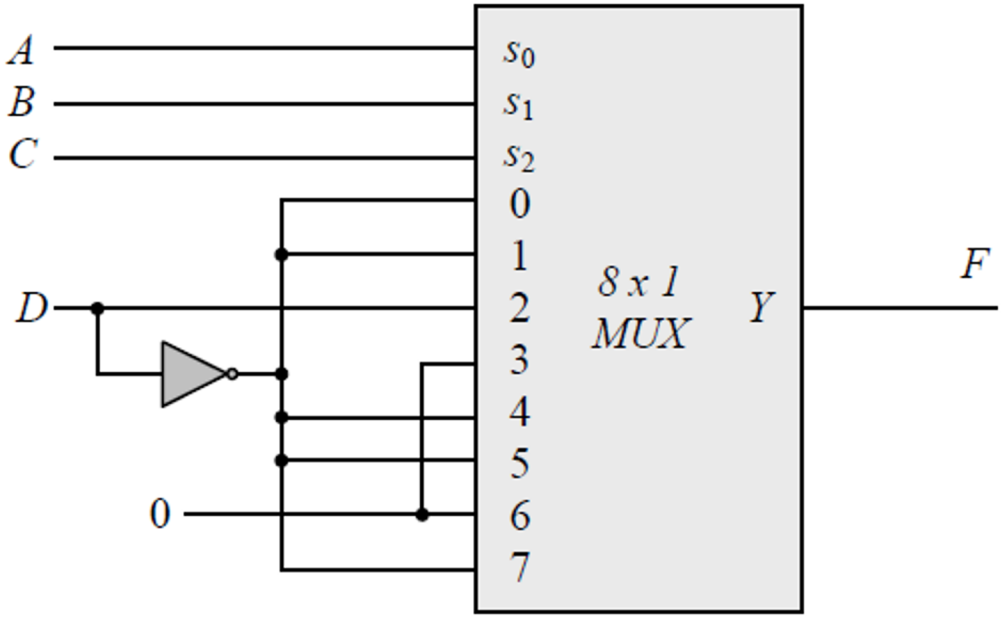
Inputs ABCD	*Mux input line (ABC)*	*Value*
000 0	0	**0**
000 1	0	1
001 0	1	**2**
001 1	1	3
010 0	2	4
010 1	2	**5**
011 0	3	6
011 1	3	7
100 0	4	**8**
100 1	4	9
101 0	5	**10**
101 1	5	11
110 0	6	12
110 1	6	13
111 0	7	**14**
111 1	7	15

Q10 $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

Inputs ABCD	*Mux input line (ABC)*	*Value*	$F = \Sigma(0, 2, 5, 8, 10, 14)$
000 0	0	**0**	1 $F = D'$
000 1	0	1	0
001 0	1	**2**	1 $F = D'$
001 1	1	3	0
010 0	2	4	0 $F = D$
010 1	2	**5**	1
011 0	3	6	0 $F = 0$
011 1	3	7	0
100 0	4	**8**	1 $F = D'$
100 1	4	9	0
101 0	5	**10**	1 $F = D'$
101 1	5	11	0
110 0	6	12	0 $F = 0$
110 1	6	13	0
111 0	7	**14**	1 $F = D'$
111 1	7	15	0

Q10 $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

Inputs ABCD	*Mux input line (ABC)*	*Value*	$F = \Sigma(0, 2, 5, 8, 10, 14)$
000 0	0	**0**	1 $F = D'$
000 1	0	1	0
001 0	1	**2**	1 $F = D'$
001 1	1	3	0
010 0	2	4	0 $F = D$
010 1	2	**5**	1
011 0	3	6	0 $F = 0$
011 1	3	7	0
100 0	4	**8**	1 $F = D'$
100 1	4	9	0
101 0	5	**10**	1 $F = D'$
101 1	5	11	0
110 0	6	12	0 $F = 0$
110 1	6	13	0
111 0	7	**14**	1 $F = D'$
111 1	7	15	0



Q11

Implement the following Boolean function with a 4x1 multiplexer and external gates.

$$F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

Q11

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$$F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

Inputs *ABCD*
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

Q11

Implement the following Boolean function with a 4x1 multiplexer and external gates.

$$F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

Inputs ABCD	*F*
0000	0
0001	1
0010	0
0011	1
0100	1
0101	0
0110	0
0111	0
1000	0
1001	0
1010	0
1011	1
1100	1
1101	1
1110	1
1111	1

Q11

Implement the following Boolean function with a 4x1 multiplexer and external gates.

$$F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

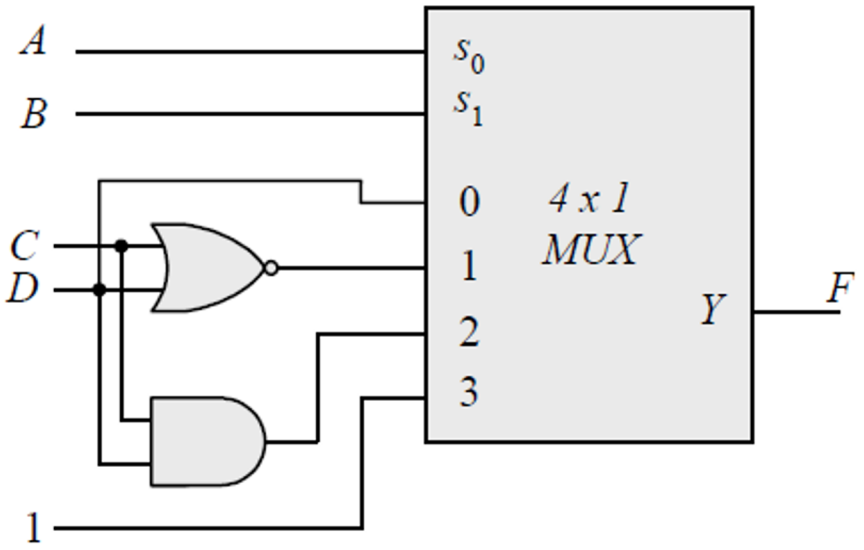
Inputs ABCD	*F*	
0000	0	
0001	1	$AB = 00$
0010	0	$F = D$
0011	1	
0100	1	
0101	0	$AB = 01$
0110	0	$F = C'D'$
0111	0	$= (C + D)'$
1000	0	
1001	0	$AB = 10$
1010	0	$F = CD$
1011	1	
1100	1	
1101	1	$AB = 11$
1110	1	$F = 1$
1111	1	

Q11

Implement the following Boolean function with a 4x1 multiplexer and external gates.

$$F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

Inputs ABCD	F	
0000	0	
0001	1	$AB = 00$
0010	0	$F = D$
0011	1	
0100	1	
0101	0	$AB = 01$
0110	0	$F = C'D'$
0111	0	$= (C + D)'$
1000	0	
1001	0	$AB = 10$
1010	0	$F = CD$
1011	1	
1100	1	
1101	1	$AB = 11$
1110	1	$F = 1$
1111	1	



Q12

Exercise 2.24 A circuit has four inputs and two outputs. The inputs, $A_{3:0}$, represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. Give simplified Boolean equations for each output and sketch a circuit.

Q12

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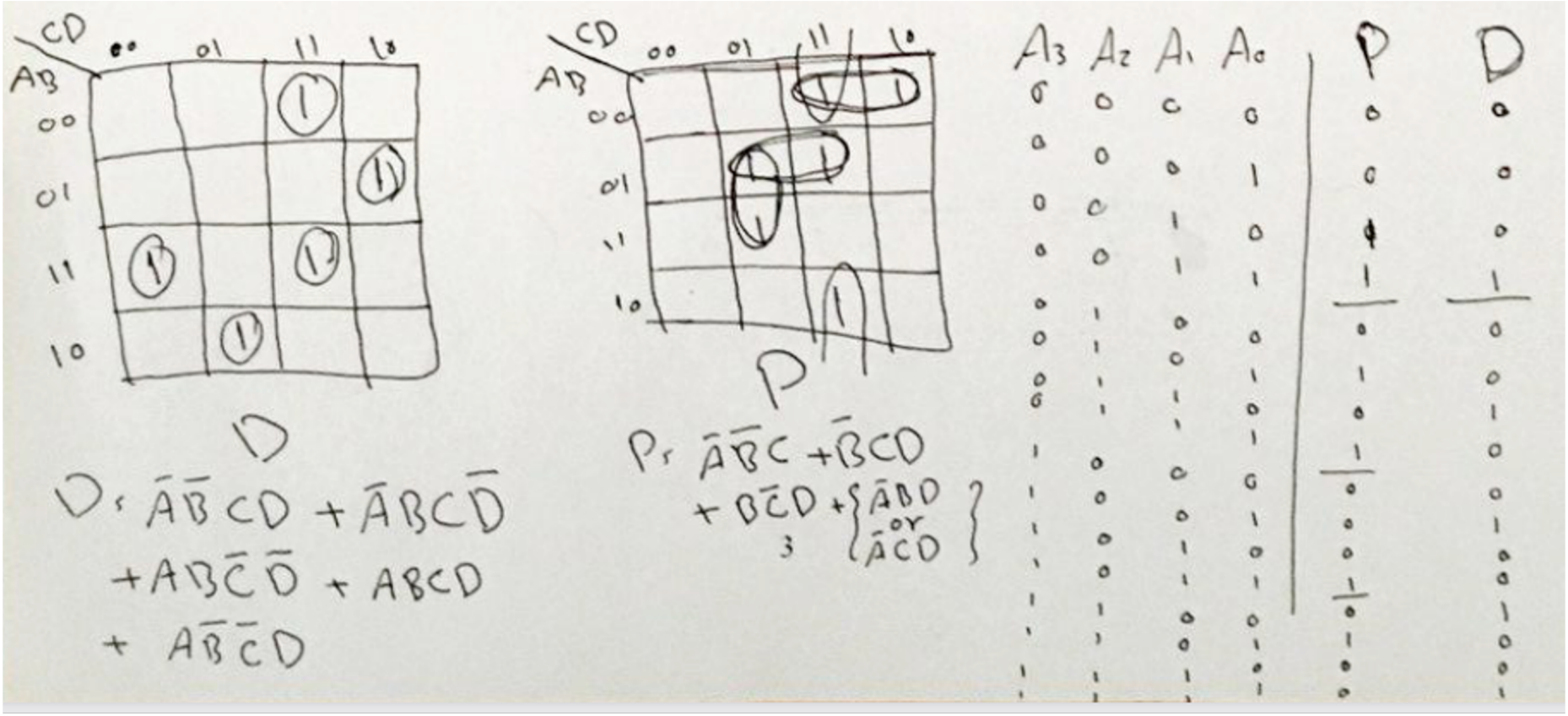
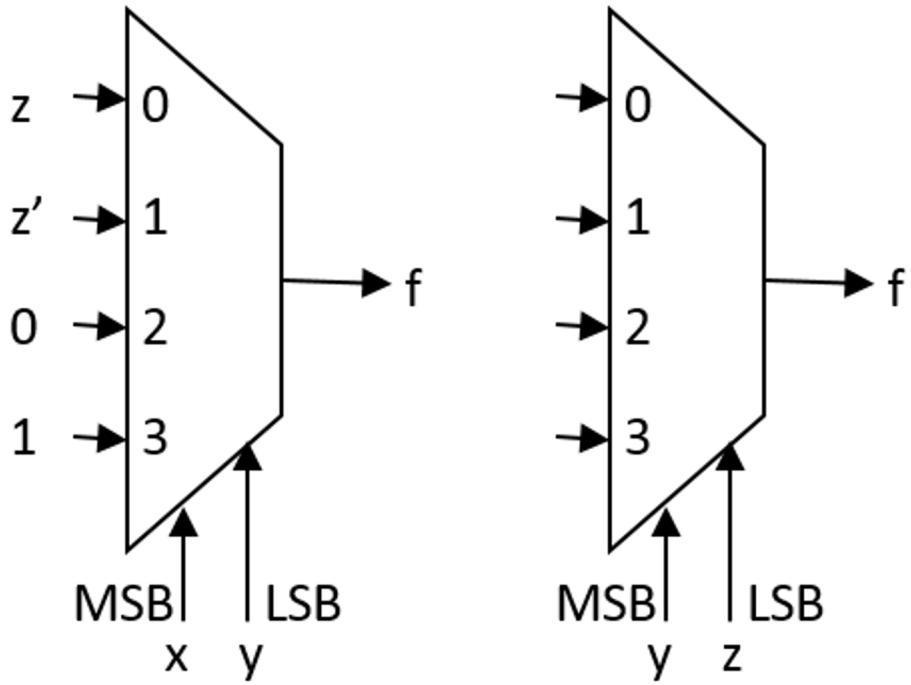
Exercise 2.24 A circuit has four inputs and two outputs. The inputs, $A_{3:0}$, represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. Give simplified Boolean equations for each output and sketch a circuit.



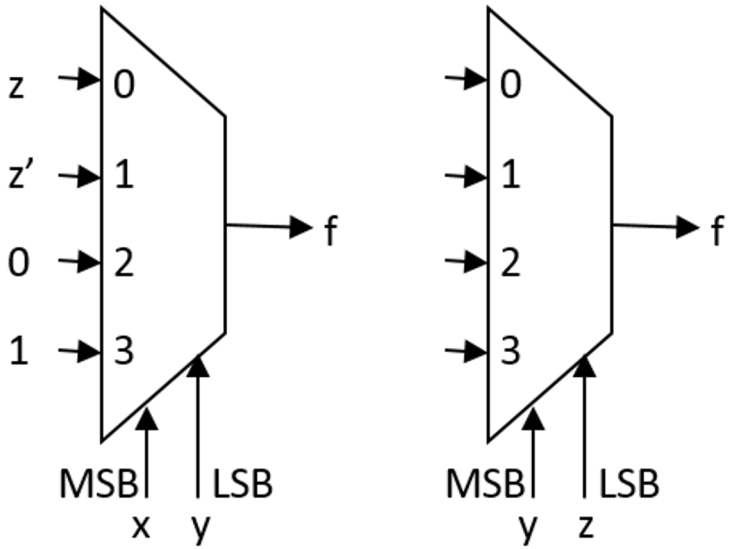
Q1 3

Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



Q1 3

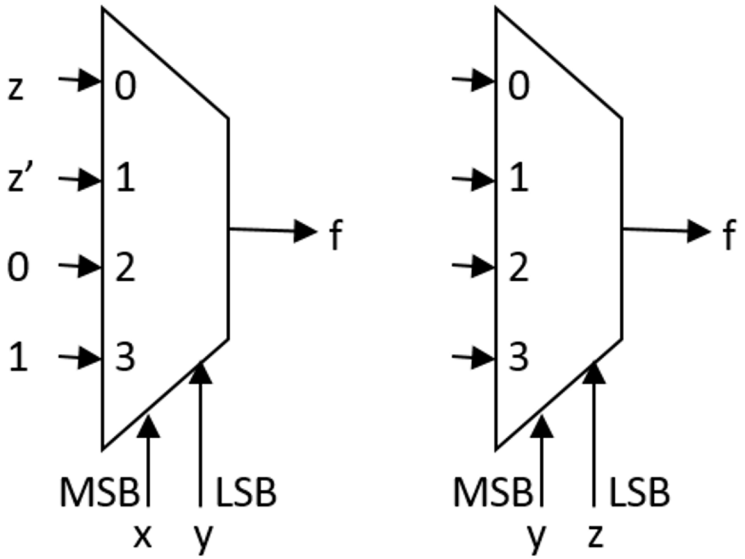
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



x	y	z	input	F	F
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Q1 3

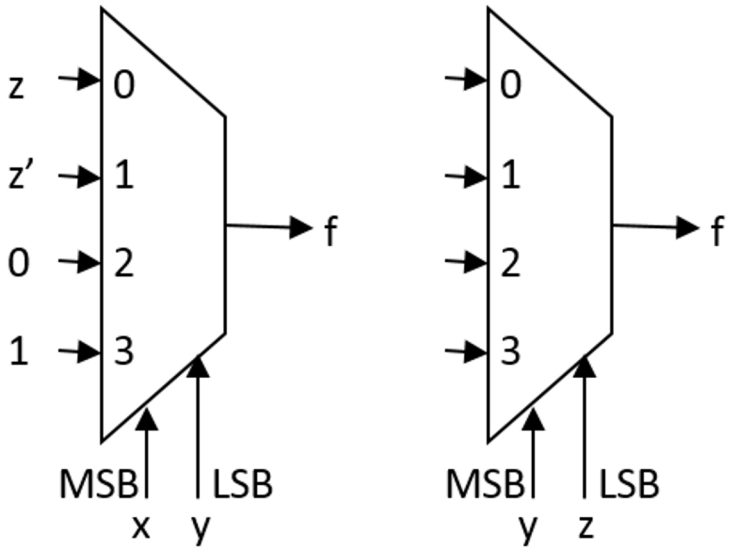
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



x	y	z	input	F	F
0	0	0	0		
0	0	1			
0	1	0	1		
0	1	1			
1	0	0	2		
1	0	1			
1	1	0	3		
1	1	1			

Q1 3

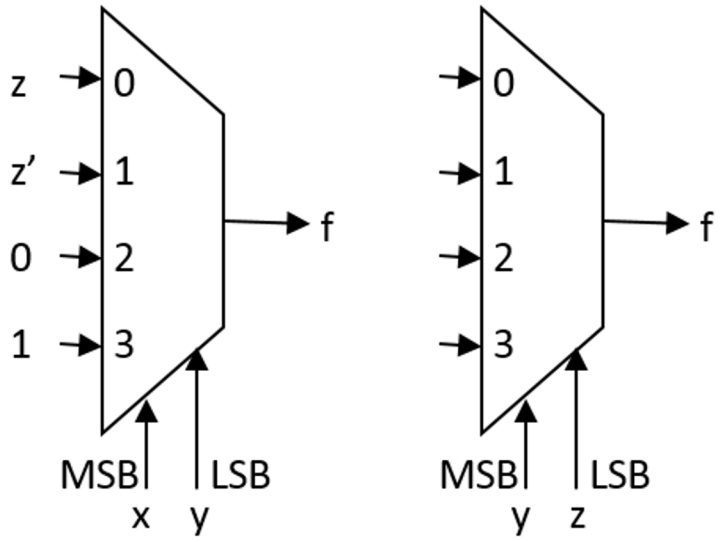
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



x	y	z	input	F	F
0	0	0	0	z	
0	0	1			
0	1	0	1	z'	
0	1	1			
1	0	0	2	0	
1	0	1			
1	1	0	3	1	
1	1	1			

Q1 3

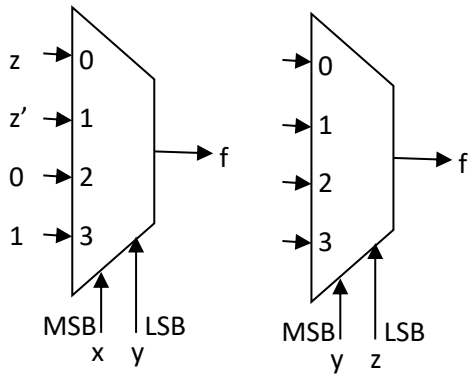
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



x	y	z	input	F	F
0	**0**	**0**	0	z	0
0	**0**	**1**			1
0	**1**	**0**	1	z'	1
0	**1**	**1**			0
1	**0**	**0**	2	0	0
1	**0**	**1**			0
1	**1**	**0**	3	1	1
1	**1**	**1**			1

Q1 3

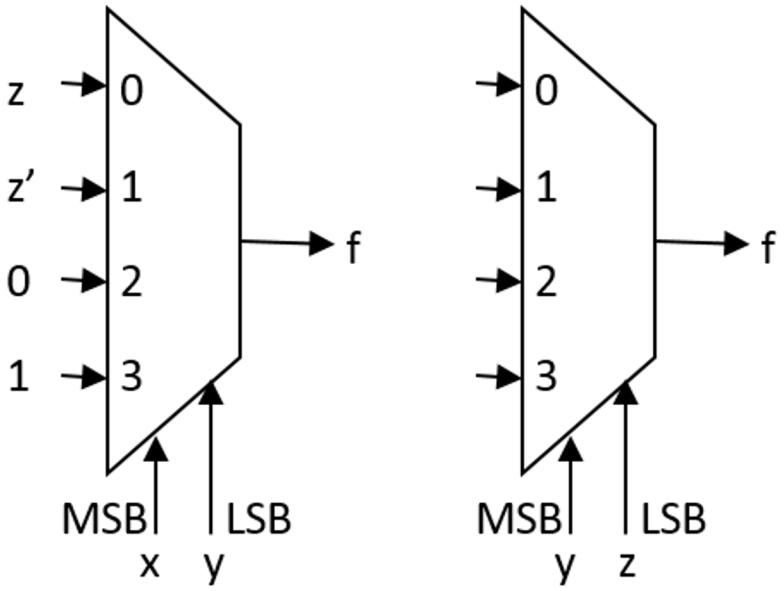
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



x	y	z	input	F	F
0	0	0	0	z	0
0	0	1			1
0	1	0	1	z'	1
0	1	1			0
1	0	0	2	0	0
1	0	1			0
1	1	0	3	1	1
1	1	1			1

Q1 3

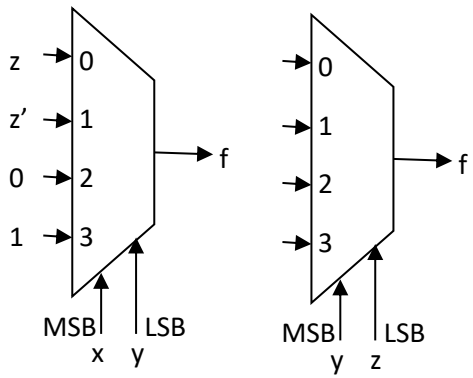
Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



y	z	x	input	F	F
0	0	0	0		
0	0	1			
0	1	0	1		
0	1	1			
1	0	0	2		
1	0	1			
1	1	0	3		
1	1	1			

Q1 3

Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.

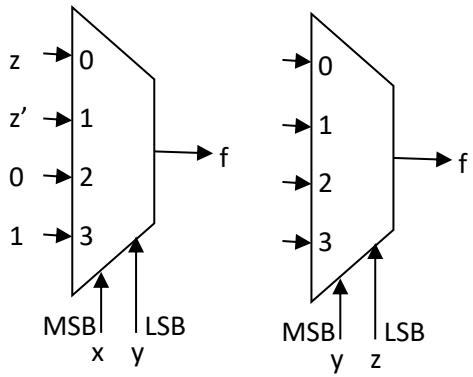


y	z	x	input	F	F
0	0	0	0		0
0	0	1			0
0	1	0	1		1
0	1	1			0
1	0	0	2		1
1	0	1			1
1	1	0	3		0
1	1	1			1

x	y	z	input	F	F
0	0	0	0	z	0
0	0	1			1
0	1	0	1	z'	1
0	1	1			0
1	0	0	2	0	0
1	0	1			0
1	1	0	3	1	1
1	1	1			1

Q1 3

Find the Boolean functions that need to be applied to the inputs of the circuit on the right in order to obtain the same function in terms of x, y, and z at the output of the circuit shown on the left.



y	z	x	input	F	F
0	0	0	0	0	0
0	0	1			0
0	1	0	1	x'	1
0	1	1			0
1	0	0	2	1	1
1	0	1			1
1	1	0	3	x	0
1	1	1			1

x	y	z	input	F	F
0	0	0	0	z	0
0	0	1			1
0	1	0	1	z'	1
0	1	1			0
1	0	0	2	0	0
1	0	1			0
1	1	0	3	1	1
1	1	1			1

Q1
4

Implement a full adder using two 4to1 multiplexers.

Q1
4

A	B	C	Carry	
0	0	0	0	0
0	0	1	0	
0	1	0	0	C
0	1	1	1	
1	0	0	0	C
1	0	1	1	
1	1	0	1	1
1	1	1	1	

Q1 4

a	b	c	Sum	
0	0	0	0	C
0	0	1	1	
0	1	0	1	C'
0	1	1	0	
1	0	0	1	C'
1	0	1	0	
1	1	0	0	C
1	1	1	1	

Q1
4