Synchronous Sequential Logic
Part I

Mantıksal Tasarım – BBM231

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Sequential Logic

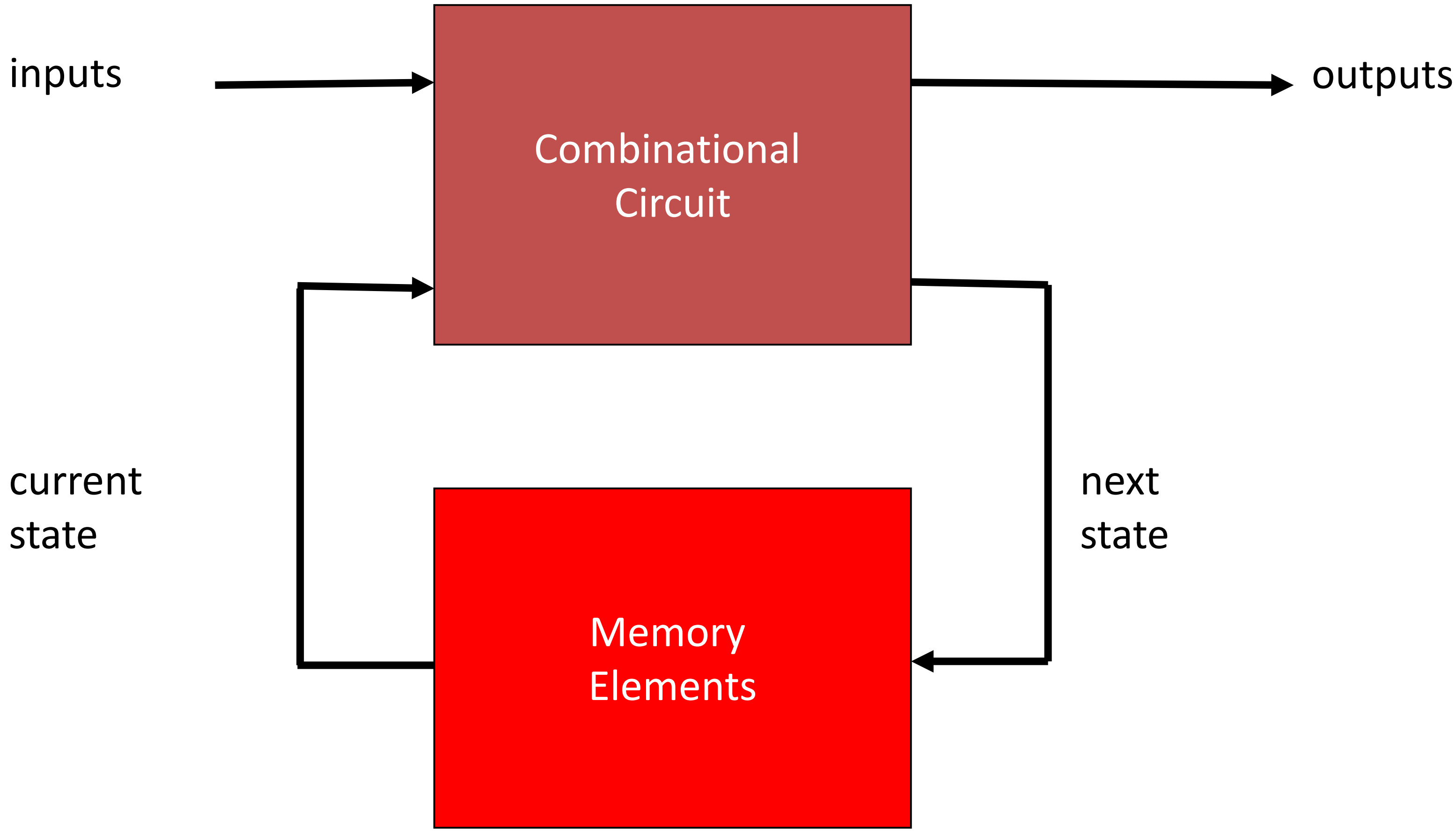
- Digital circuits we have learned, so far, have been **combinational**

  >> no memory,

  >> outputs are entirely defined by the “current” inputs

- However, many digital systems encountered in everyday life are **sequential** (i.e. **they have memory**)
  - **the memory elements remember past inputs**
  - **outputs of sequential circuits are not only dependent on the current input but also the state of the memory elements.**

Sequential Circuits Model



current state is a function of **past inputs + initial state**

Classification

There are 2 types of sequential circuits

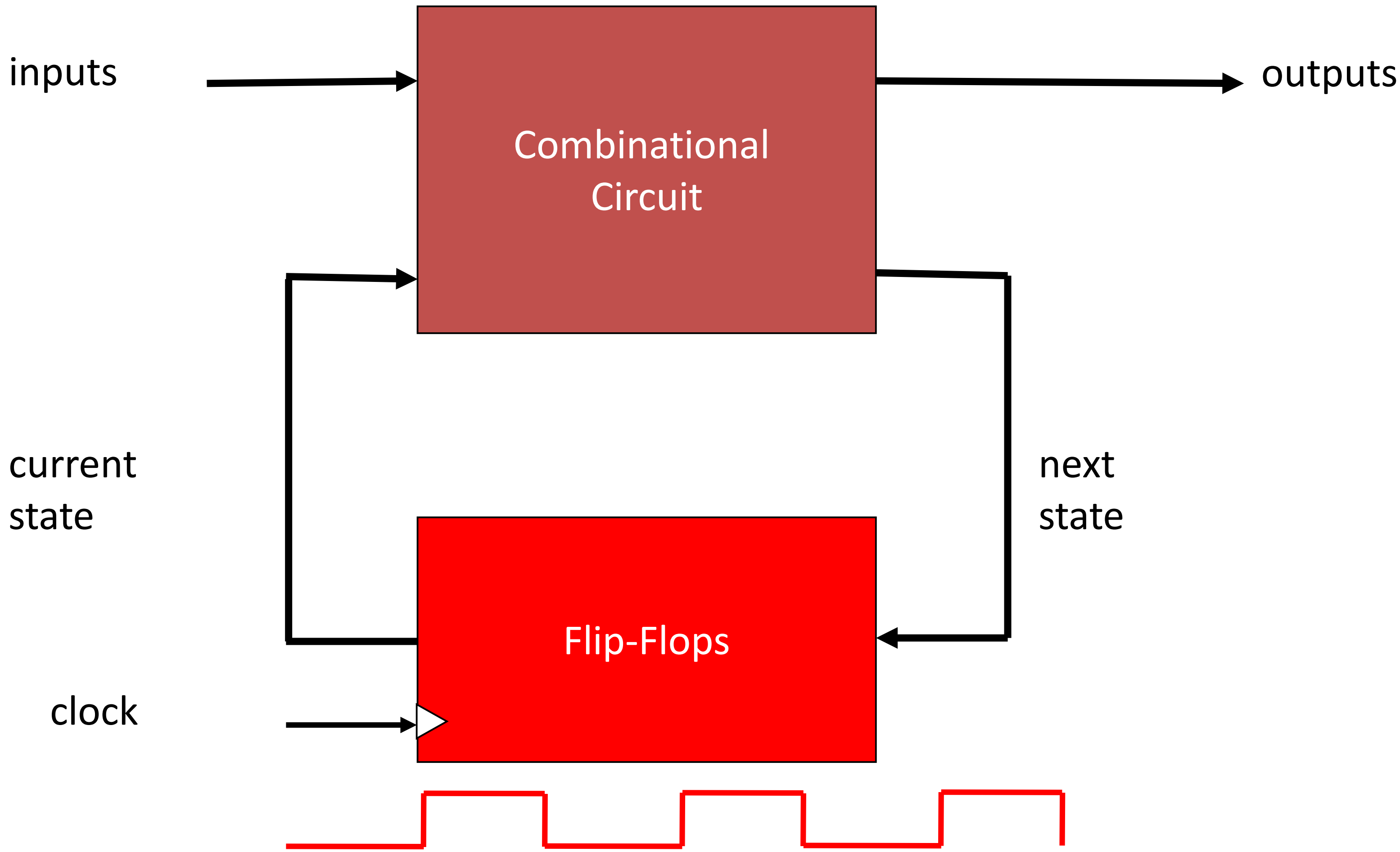
1. Synchronous
   - Signals affect the memory elements at discrete instants of time.
   - Discrete instants of time requires synchronization.
   - Synchronization is usually achieved through the use of a common clock.
   - A "clock generator" is a device that generates a periodic train of pulses.

Classification

1. Synchronous
   - The state of the memory elements are updated with the arrival of each pulse
   - This type of logical circuit is also known as <u>clocked sequential</u> circuits.
2. Asynchronous
   - No clock
   - Behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.
   - Memory elements in asynchronous circuits are regarded as time-delay elements

Clocked Sequential Circuits

- Memory elements are flip-flops which are logic devices, each of which is capable of storing one bit of information.



Clocked Sequential Circuits

- The outputs of a clocked sequential circuit can come from
  - the combinational circuit,
  - the outputs of the flip-flops
  - or both.
- The state of the flip-flops can change only during a clock pulse transition
  - i.e. low-to-high and high-to-low
  - clock edge
- When the clock maintains its value, the flip-flop output does not change
- The transition from one state to the next occurs at the clock edge.

Machine

Machine (

Inputs {X},

States {D},

Outputs {Z},

Output Function {F : $X \times D \rightarrow Z$},

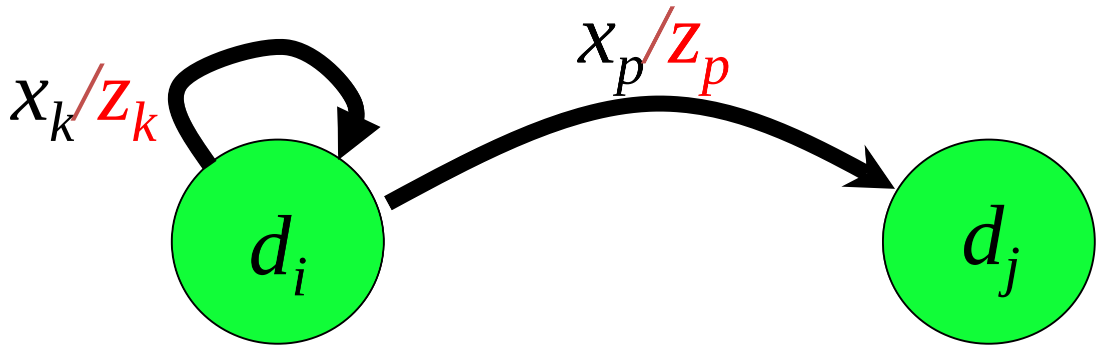
Next State Function {G : $X \times D \rightarrow D$}

)

Representation with **State Diagram**

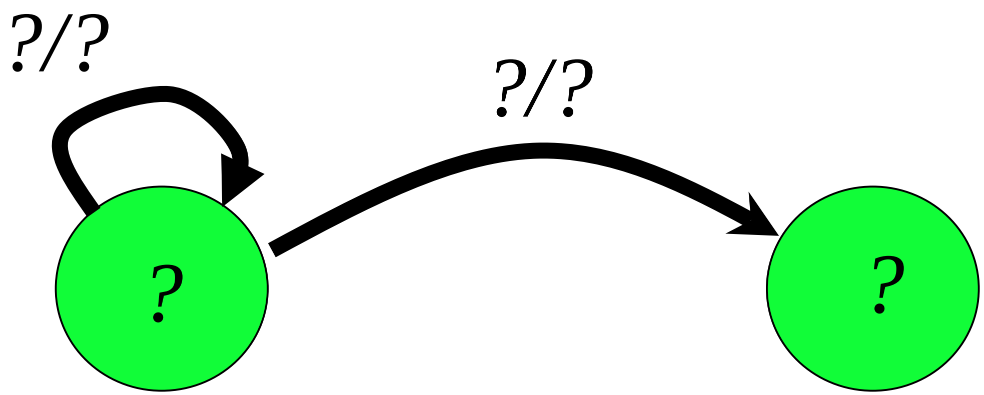
	x_1	x_2	$\ldots$	x_i	$\ldots$	x_l
d_1						
d_2						
$\vdots$						
d_i				d_j, z		
$\vdots$						
d_{r-1}						
d_r						

Assign a Node to Each State



- Machine is at state d_i , input x_k comes, the next state will be again d_i and the output is z_k
- Machine is at state d_i , input x_p comes, the next state will be d_j and the output is z_p

Assign a Node to Each State



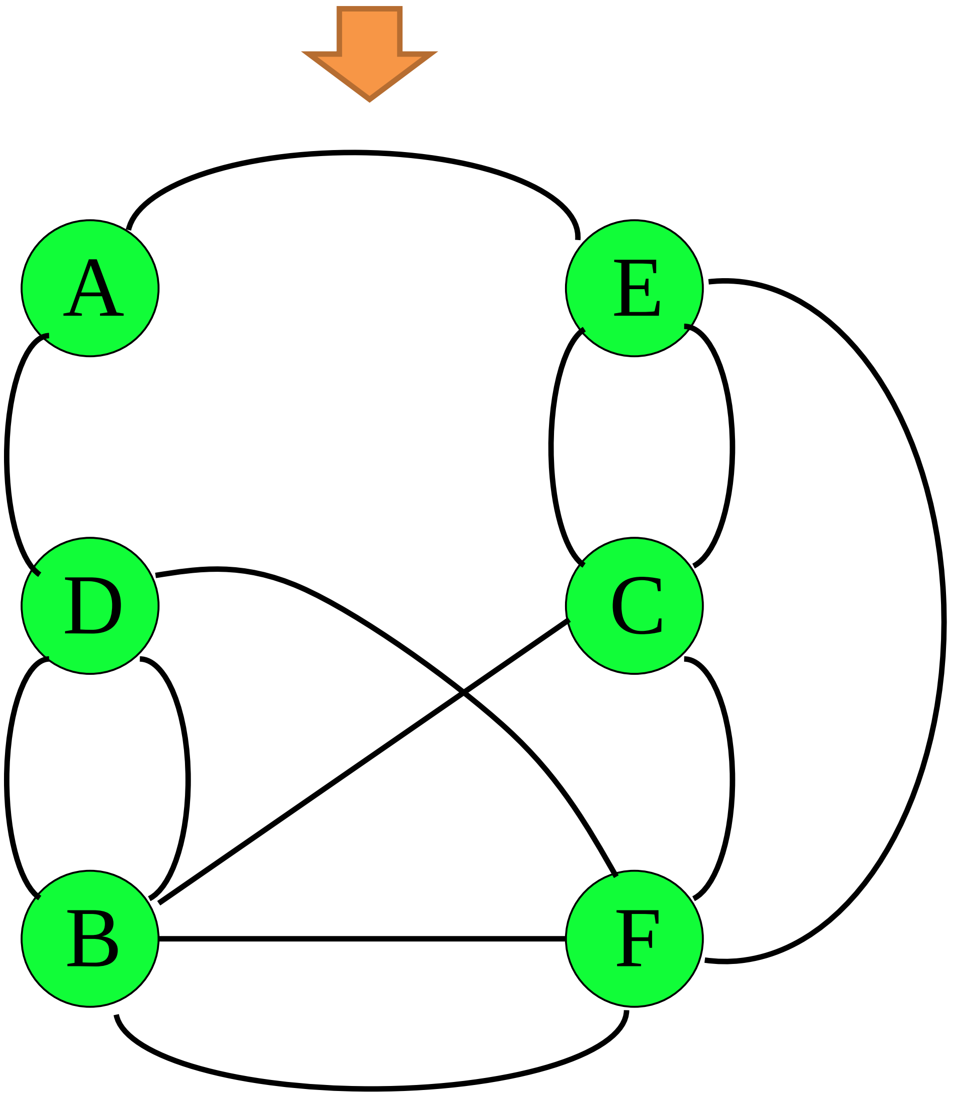
- Machine is at state d_m, input x_t comes, the next state will be again d_m and the output is z_t
- Machine is at state d_m, input x_u comes, the next state will be d_n and the output is z_u

Notation

- Let $\mathbf{I_k}$ be an **input sequence** with length equal to k, i.e. $I_k = x_1x_2\ldots x_k$
- $\mathbf{f(I_k,d_i)} = z_1z_2\ldots z_k$ is an **output sequence**
- $\mathbf{g(I_k,d_i)} = d_{i1}d_{i2}\ldots d_{ik}$ is a **state sequence**
- $d_i \xrightarrow{I_k} \mathbf{d_{ik}}$: **Follower of $\mathbf{d_i}$** after the input sequence I_k

Example - Fill out the rest

	0	1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0



Example

	0	1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

- Let I_5=10110, find $g(I_5,C)$ and $f(I_5,C)$

I_5						
$g(I_5,C)$						
$f(I_5,C)$						

- I_5 follower of C : ?

Example

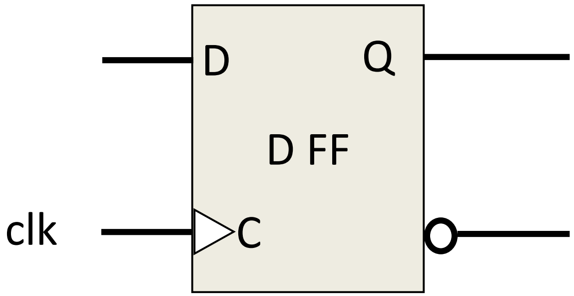
	0	1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

- Let I_5=10110, find $g(I_5,C)$ and $f(I_5,C)$

I_5		1	0	1	1	0
$g(I_5,C)$	C	B	F	C	B	F
$f(I_5,C)$		1	0	0	1	0

- I_5 follower of C is F

D Flip-Flop



Positive edge-triggered
D Flip-Flop

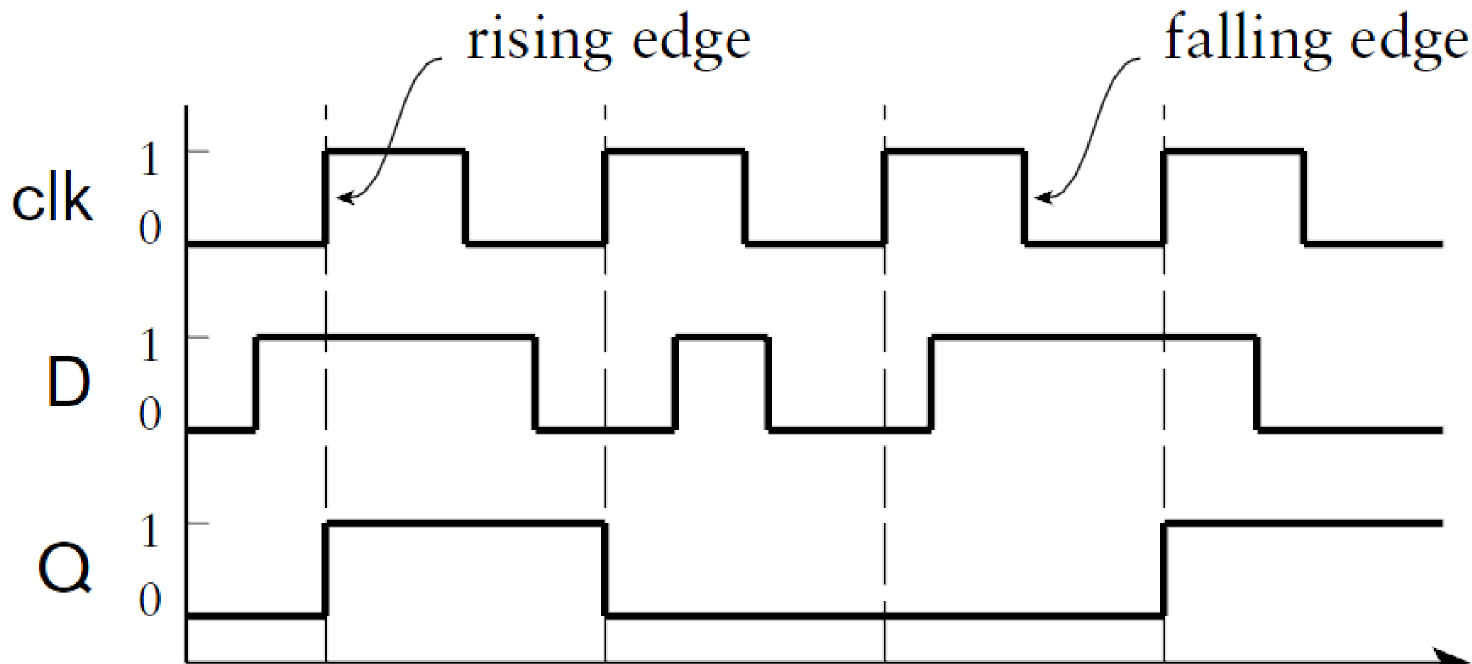
- **Characteristic equation**

  $Q(t+1) = D$

D	Q(t+1)
0	0
1	1

Characteristic Table

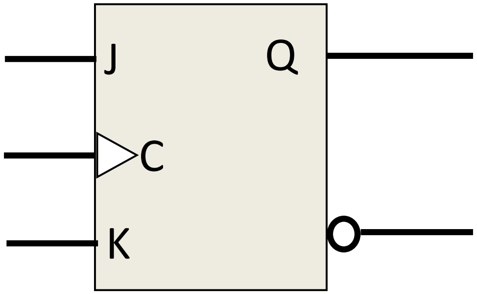
Timing Diagram of D Flip-Flop



Other Flip-Flops

- D flip-flop is the most common
  - since it requires the fewest number of gates to construct.
- Two other widely used flip-flops
  - JK flip-flops
  - T flip-flops
- JK flip-flops
  - Three FF operations
    1. Set
    2. Reset
    3. Complement

JK Flip-Flops

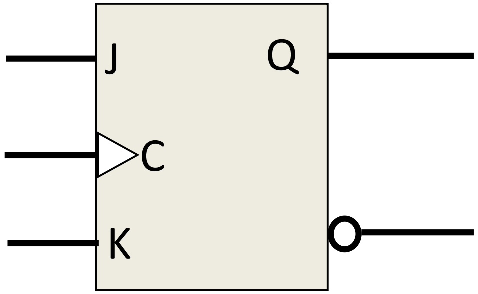


J	K	Q(t+1)	next state
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Characteristic Table

Characteristic Equation of JK flip-flop?

JK Flip-Flops

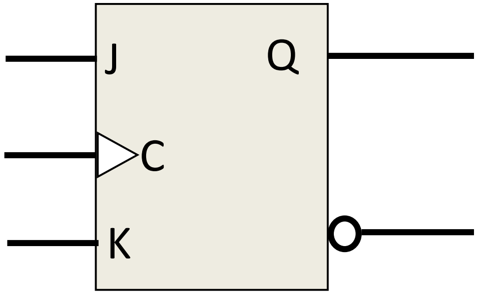


J	K	Q(t+1)	next state
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Characteristic Table

J	K	Q(t)	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

JK Flip-Flops



J	K	Q(t+1)	next state
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	Set
1	1	Q′(t)	Complement

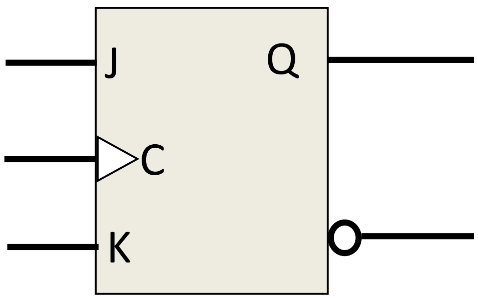
Characteristic Table

J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J \ K,Q(t)	00	01	11	10
0	0	1	0	0
1	1	1	0	1

Q(t+1) = ?

JK Flip-Flops



J	K	Q(t+1)	next state
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	Set
1	1	Q′(t)	Complement

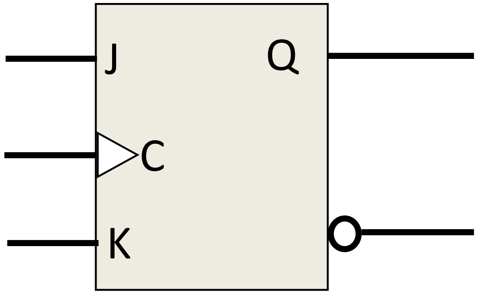
Characteristic Table

J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J \ K,Q(t)	00	01	11	10
0	0	1	0	0
1	1	1	0	1

Q(t+1) = ?

JK Flip-Flops



J	K	Q(t+1)	next state
0	0	Q(t)	no change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

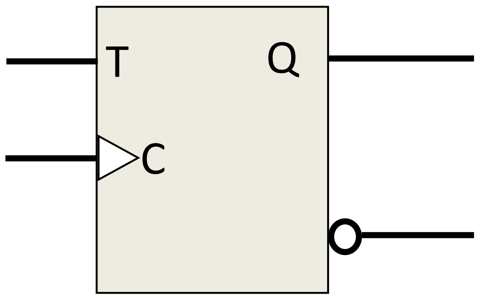
Characteristic Table

- Characteristic equation

  $Q(t+1) = JQ'(t) + K'Q(t)$

T (Toggle) Flip-Flop

- Complementing flip-flop

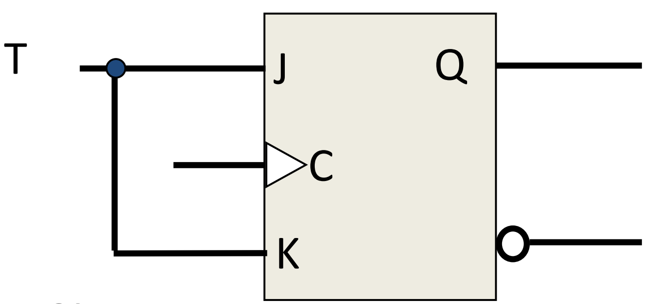


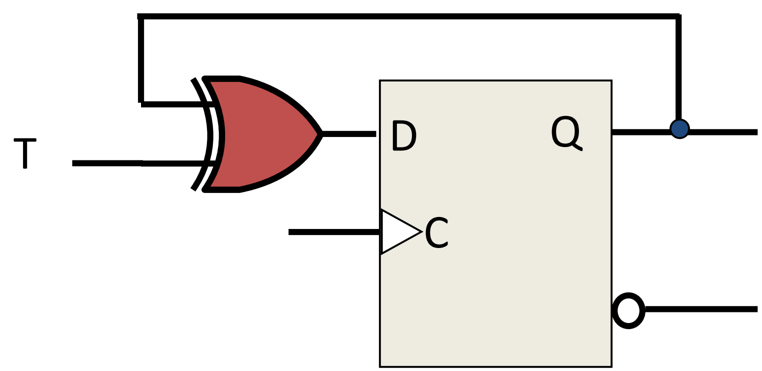
T	Q(t+1)	next state
0	Q(t)	no change
1	Q'(t)	Complement

Characteristic Table

- Characteristic equation

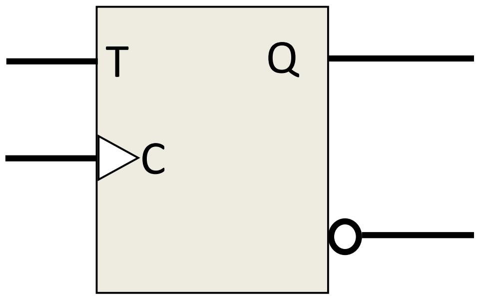
  Q(t+1) = ?





T (Toggle) Flip-Flop

- Complementing flip-flop

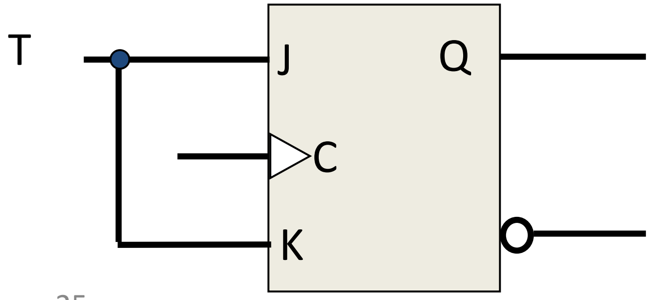


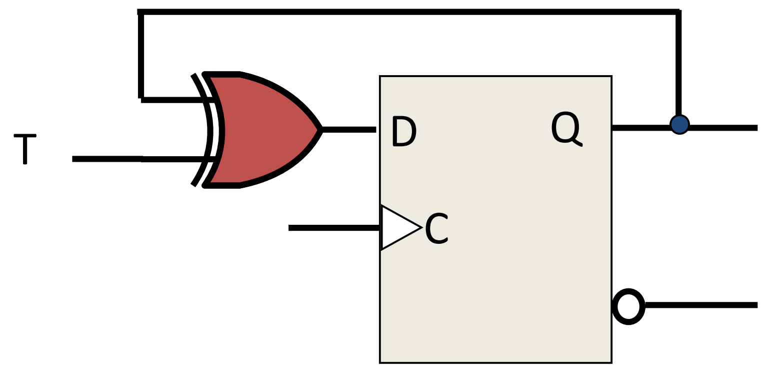
T	Q(t+1)	next state
0	Q(t)	no change
1	Q'(t)	Complement

Characteristic Table

- Characteristic equation

$Q(t+1) = Q(t) \oplus T$





Characteristic Equations

The logical properties of a flip-flop can be expressed algebraically using characteristic equations :

- D flip-flop

  $$Q(t+1) = D$$

- JK flip-flop

  $$Q(t+1) = JQ'(t) + K'Q(t)$$

- T flip-flop

  $$Q(t+1) = Q(t) \oplus T$$

What if we have Q(t+1) and Q(t), and looking for J and K values?

Q(t)Q(t+1)	00	01	11	10
J,K	0,X	1,X	X,0	X,1

$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

What if we have Q(t+1) and Q(t), and looking for D value?

Q(t)Q(t+1)	00	01	11	10
D	0	1	1	0

D= Q(t+1)

What if we have Q(t+1) and Q(t), and looking for T value?

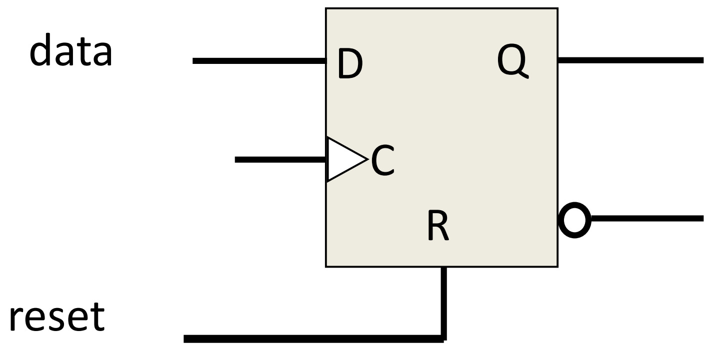
Q(t)Q(t+1)	00	01	11	10
T	0	1	0	1

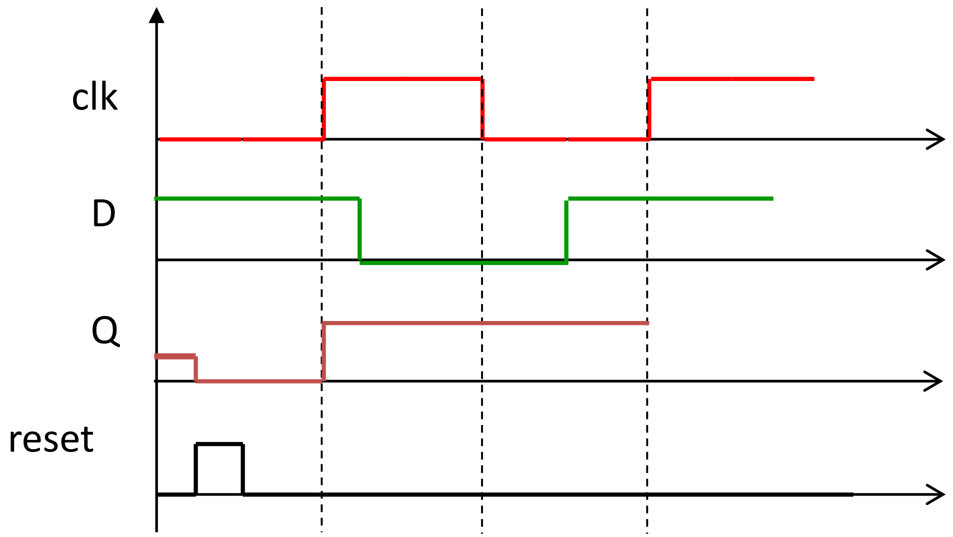
$T = Q(t) \oplus Q(t+1)$

Asynchronous Inputs of Flip-Flops

- They are used to force the flip-flop to a particular state independent of clock
  - "Preset" (direct set) set FF state to 1
  - "Clear" (direct reset) set FF state to 0
- They are especially useful at startup.
  - In digital circuits when the power is turned on, the state of flip-flops are unknown.
  - Asynchronous inputs are used to bring all flip-flops to a known "starting" state prior to clock operation.

Asynchronous Inputs



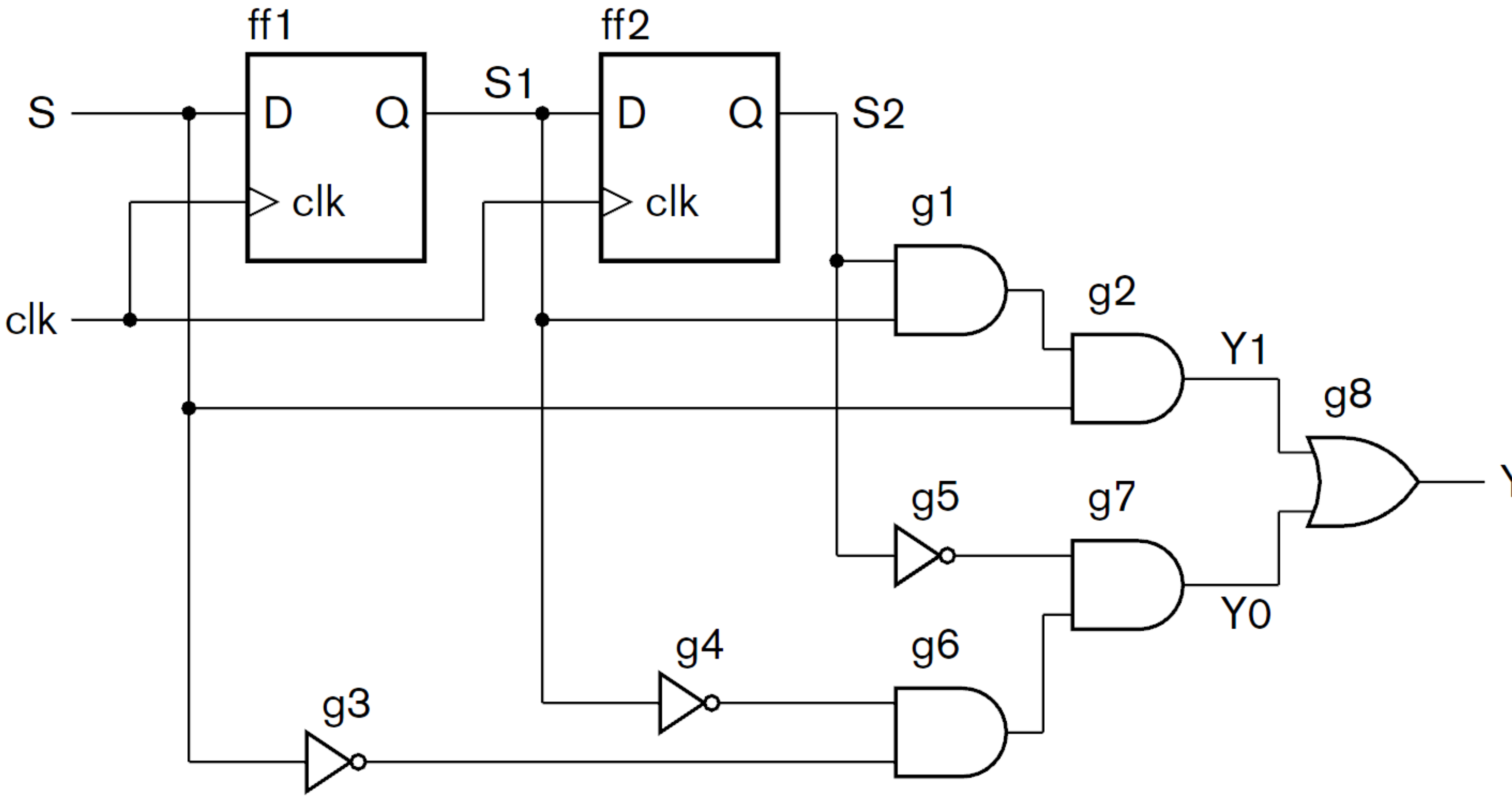


reset	C	D	Q	Q'	
1	X	X	0	1	Starting State
0	↑	0	0	1	
0	↑	1	1	0	

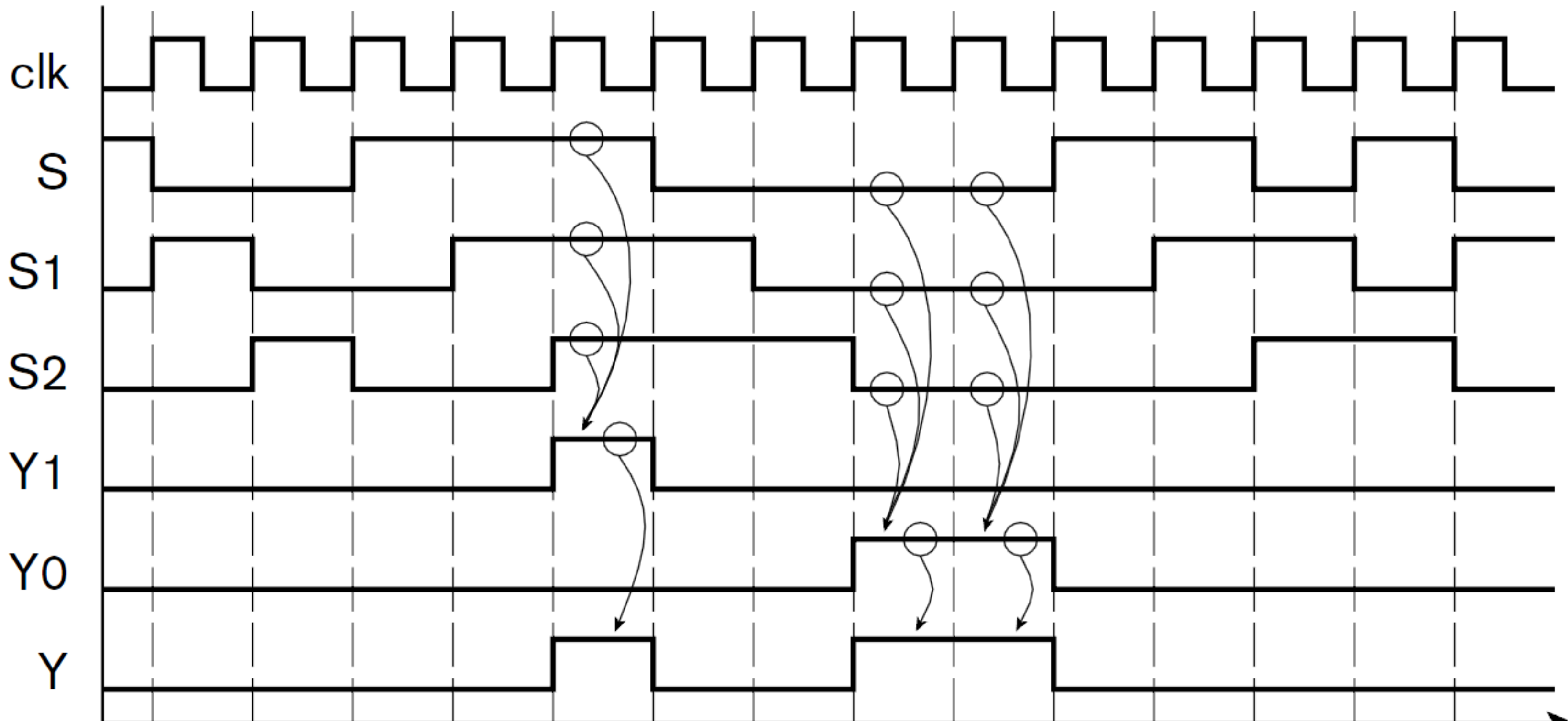
Analysis of Clocked Sequential Circuits

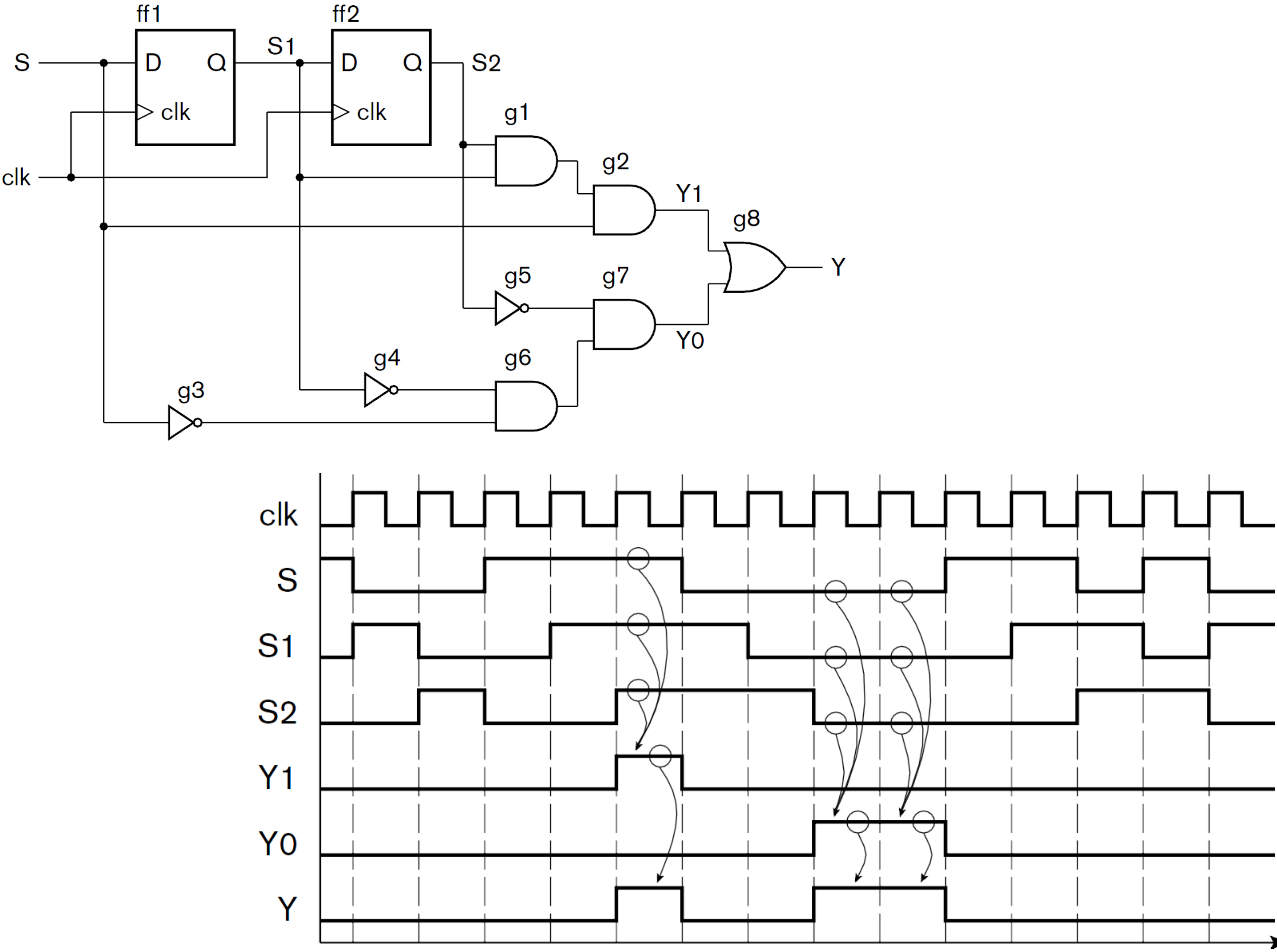
- Goal:
  - to determine the behavior of clocked sequential circuits
  - "Behavior" is determined from
    - Inputs
    - Outputs
    - State of the flip-flops
  - We have to obtain
    - Boolean expressions for output and next state
      - output & state equations
    - (state) table
    - (state) diagram

Analyze the circuit



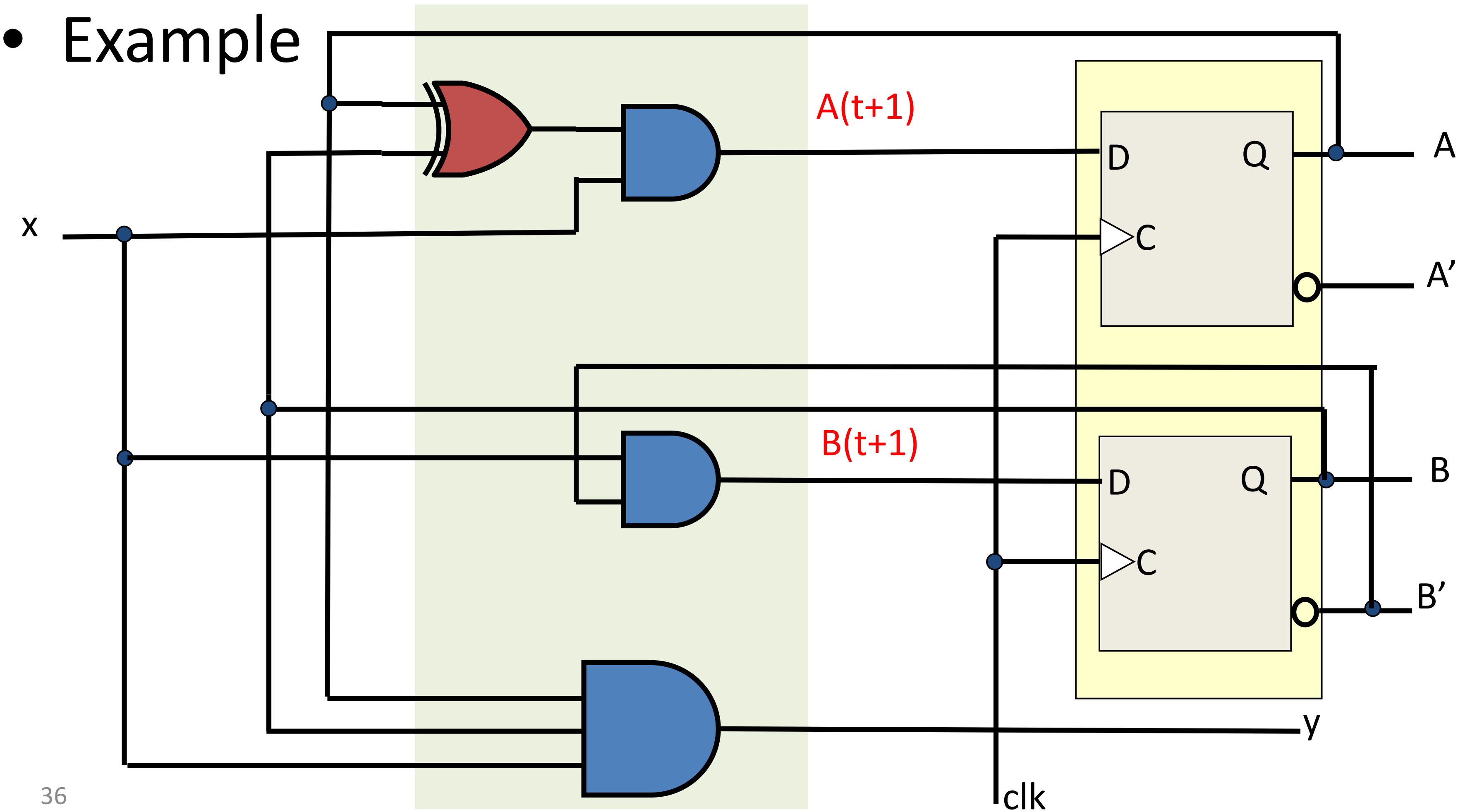
Run it and check the timing diagram




ff1
ff2
S
D
Q
clk
S1
S2
g1
g2
g3
g4
g5
g6
g7
g8
Y1
Y0
Y
clk
S
S1
S2
Y1
Y0
Y

State Equations

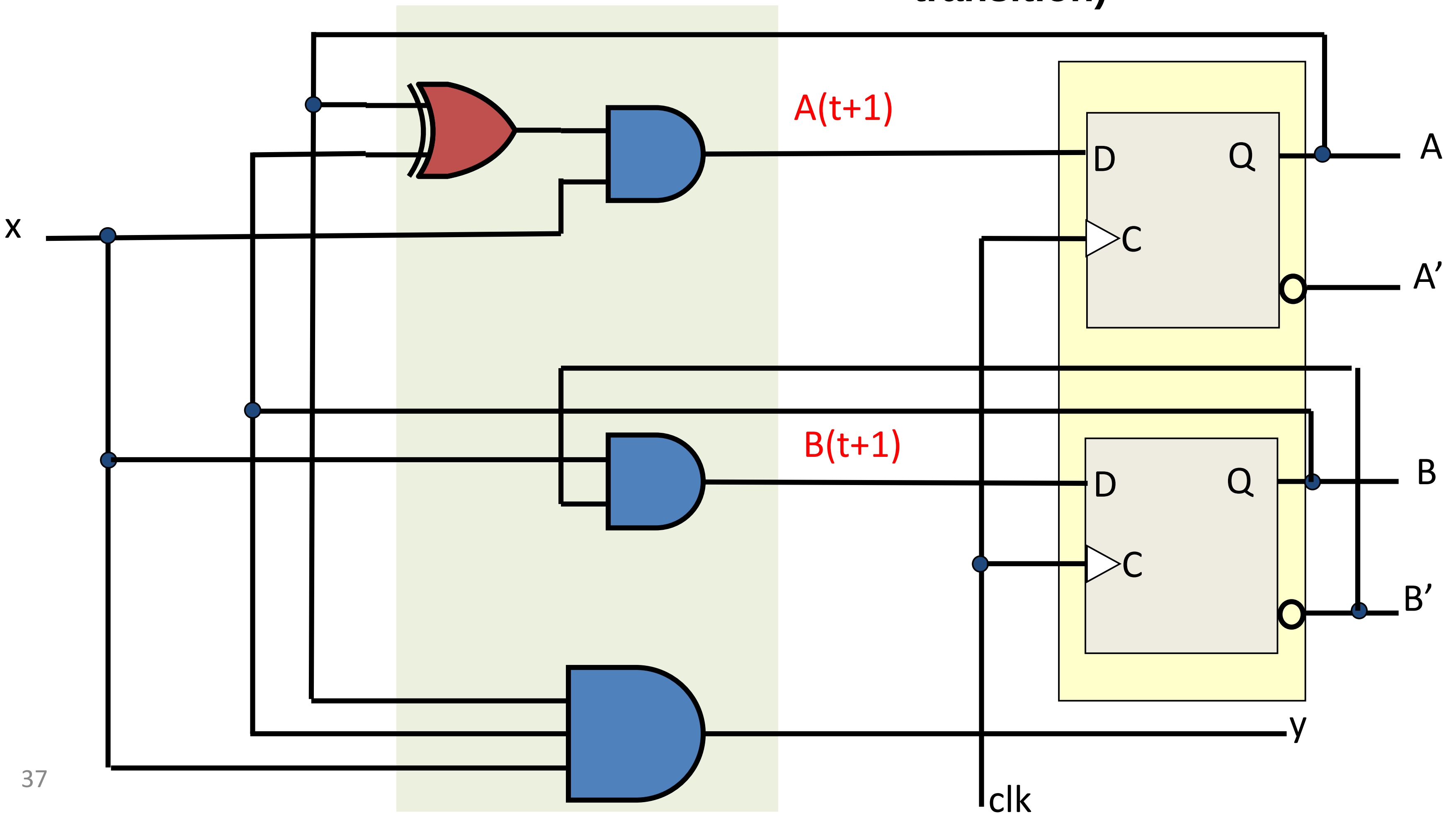
- Also known as "transition equations"
  - specify the next state as a function of the present state and inputs
- Example



Output and State Equations

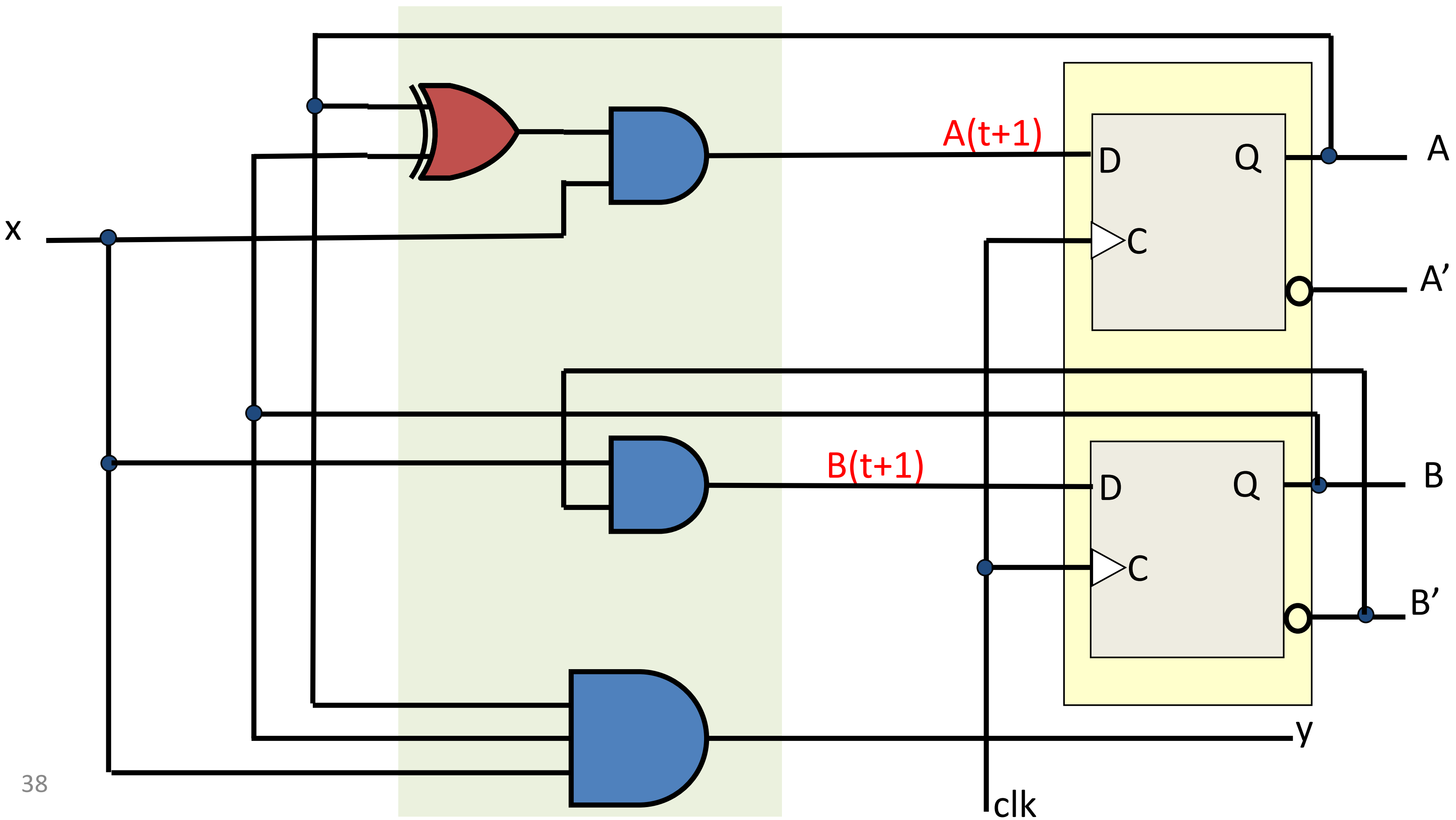
- A(t+1) =
- B(t+1) =
- y =

input of a flip-flop determines the value of the next state (i.e., the state reached after the clock transition)



Output and State Equations

- $A(t+1) = (A(t) \oplus B(t))\, x$
- $B(t+1) = (B(t))'\, x$
- $y = A(t)B(t)\, x$



Flip Flop Input Equations

- Flip-Flop input (excitation) equations
- Same as the state equations in D flip-flops

Example: State (Transition) Table

$A(t+1) = (AB' + A'B)x$ $B(t+1) = B'x$ $y = ABx$

Present state		input	Next state		output
A(t)	B(t)	x	A(t+1)	B(t+1)	y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

A sequential circuit with **m** FFs and **n** inputs needs $\mathbf{2^{m+n}}$ rows in the transition table

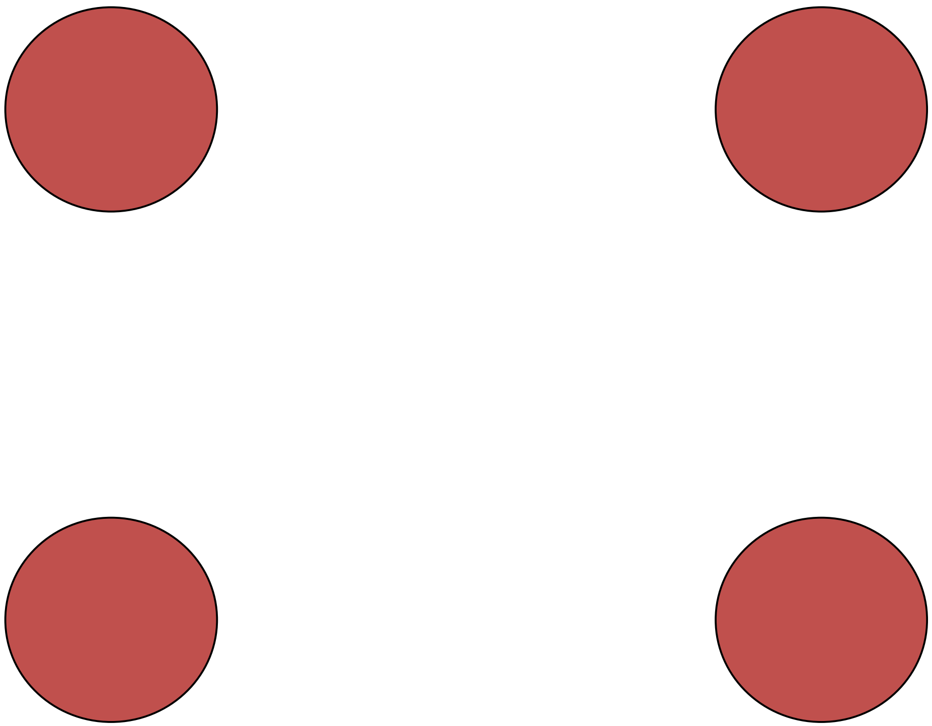
Example: State (Transition) Table

$A(t+1) = (AB' + A'B)x$ $B(t+1) = B'x$ $y = ABx$

Present state		input	Next state		output
A(t)	B(t)	x	A(t+1)	B(t+1)	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

A sequential circuit with **m** FFs and **n** inputs needs $\mathbf{2^{m+n}}$ rows in the transition table

Example: State Diagram

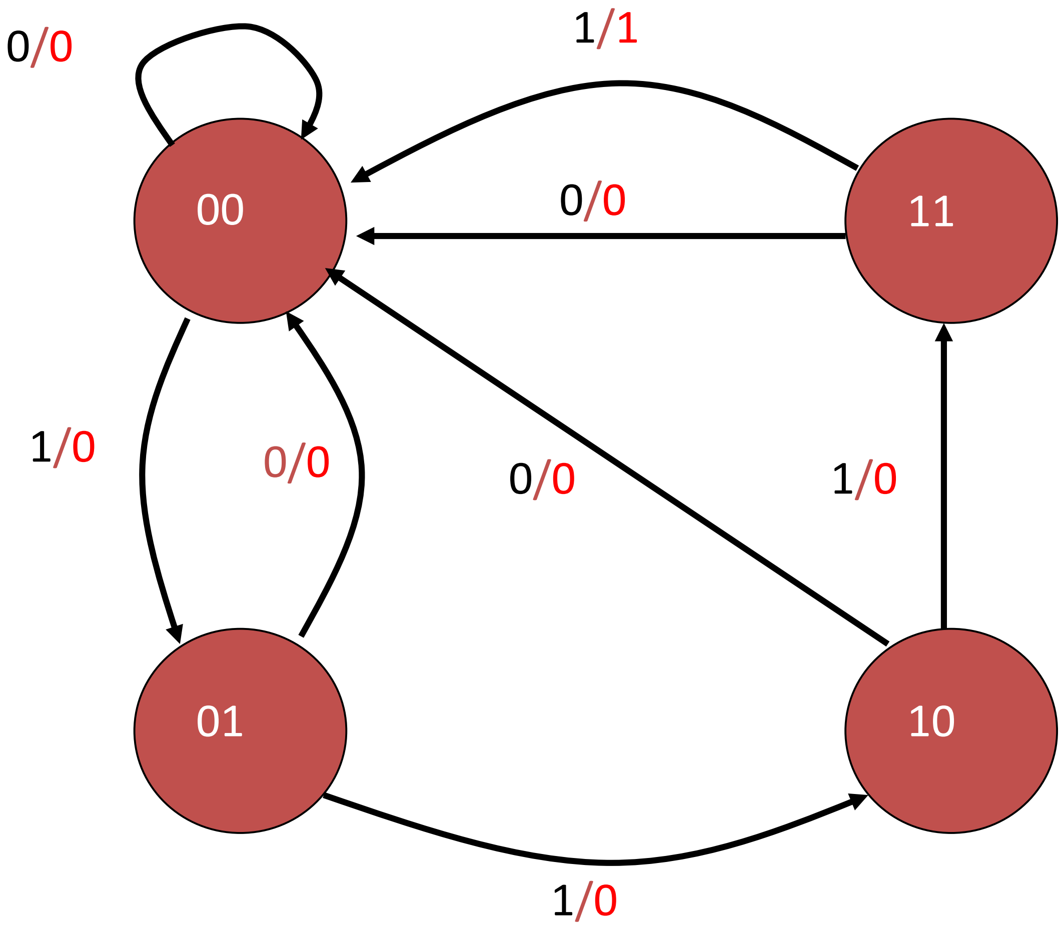


Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

What is this circuit doing?

State diagram provides the same information as state table

Example: State Diagram



Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

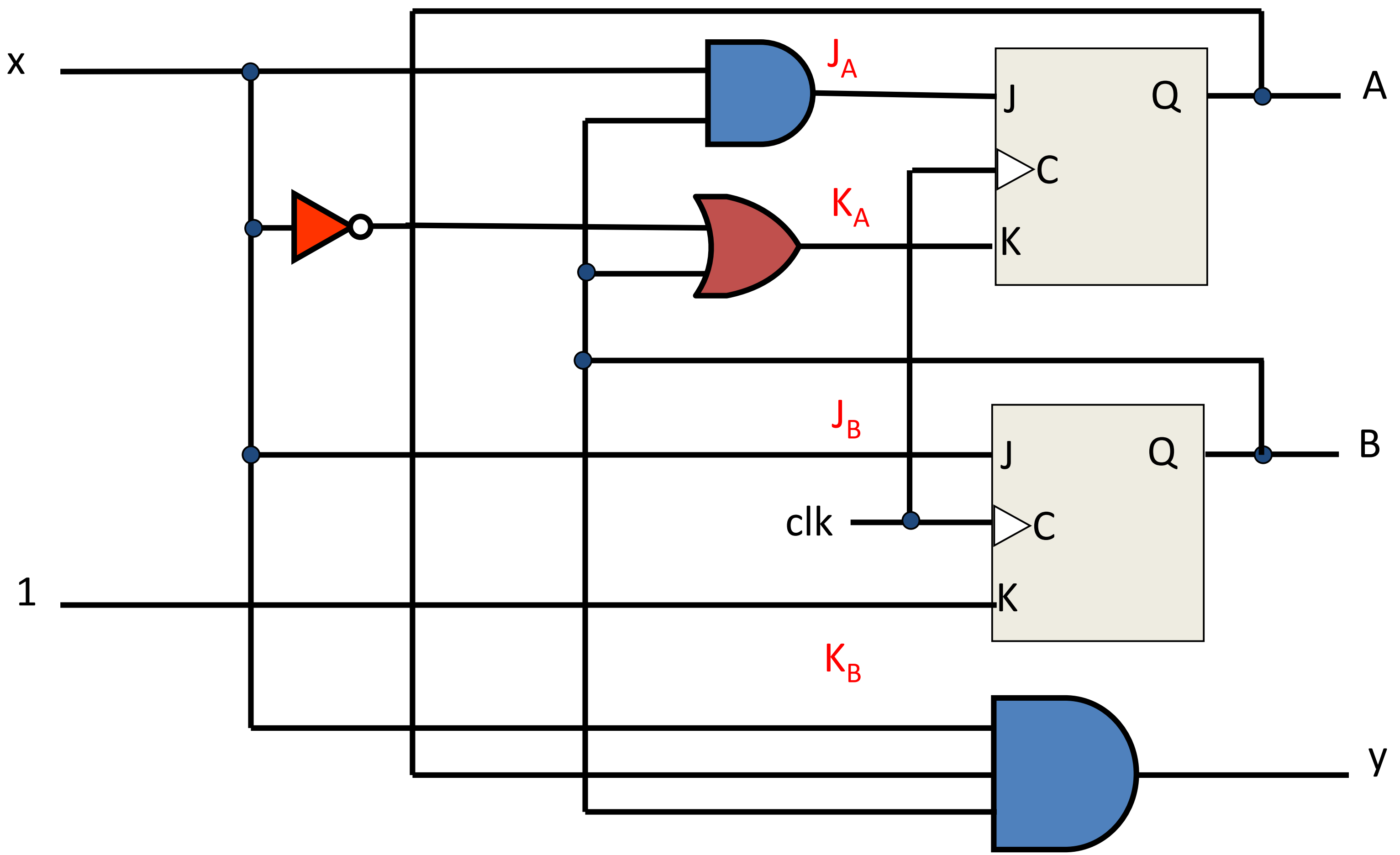
What is this circuit doing?

State diagram provides the same information as state table

Analysis with JK Flip-Flops

- For a D flip-flop, the state equation is the same as the flip-flop input equation
  - $Q(t+1) = D$
- For JK flip-flops, situation is different
  - Goal is to find state equations
  - Method
    1. Determine flip-flop input equations
    2. List the binary values of each input equation
    3. Use the corresponding flip-flop characteristic table to determine the next state values in the state table

Example: Analysis with JK FFs



- Flip-flop input equations

  $J_A =$ and $K_A =$

  $J_B =$ and $K_B =$

Example: Analysis with JK FFs

- $J_A = Bx$ and $K_A = x' + B$
- $J_B = x$ and $K_B = 1$

present State		input	next state		FF inputs			
A(t)	B(t)	x	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

Example: Analysis with JK FFs

- $J_A = Bx$ and $K_A = x' + B$
- $J_B = x$ and $K_B = 1$

Characteristic equations
- $A(t+1) = ?$
- $B(t+1) = ?$
- $y = ?$

present State		input	next state		FF inputs			
$A(t)$	$B(t)$	x	$A(t+1)$	$B(t+1)$	J_A	K_A	J_B	K_B
0	0	0	0	0	0	1	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	0	0	1	0	1
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	1	0	1
1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	0	1
1	1	1	0	0	1	1	1	1

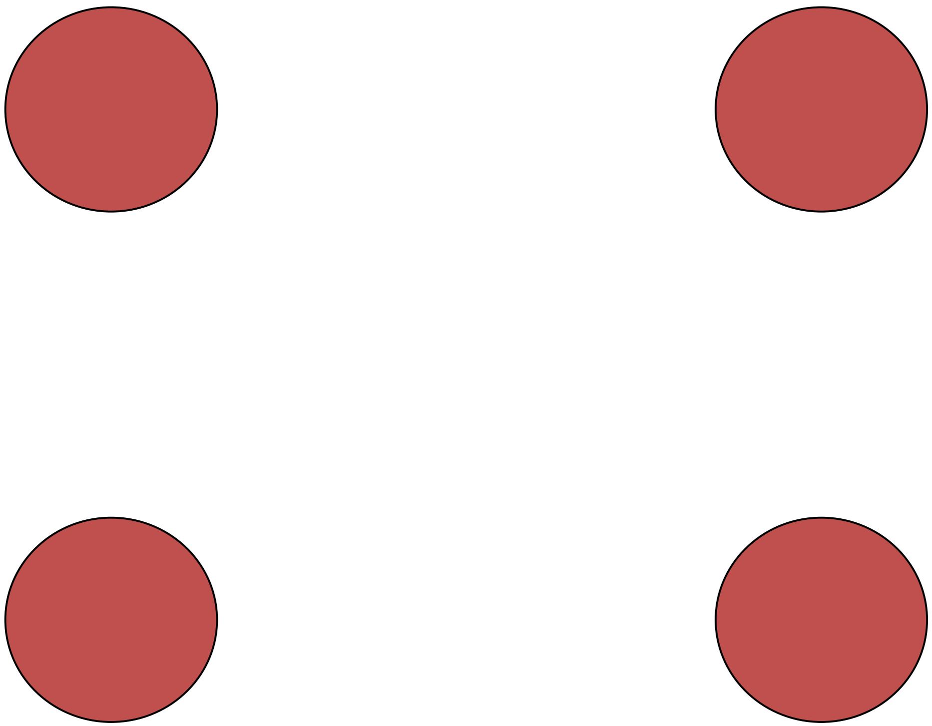
Example: Analysis with JK FFs

- Characteristic equations
  - $A(t+1) = J_A A' + K'_A A$
  - $B(t+1) = J_B B' + K'_B B$
  - $y = ABx$
- Input equations
  - $J_A = Bx$ and $K_A = x'+B$
  - $J_B = x$ and $K_B = 1$
- State equations
  - $A(t+1) =$
    $=$
  - $B(t+1) =$

Example: Analysis with JK FFs

- Characteristic equations
  - $A(t+1) = J_A A' + K'_A A$
  - $B(t+1) = J_B B' + K'_B B$
  - $y = ABx$
- Input equations
  - $J_A = Bx$ and $K_A = x'+B$
  - $J_B = x$ and $K_B = 1$
- State equations
  - $A(t+1) = A'Bx + (x'+B)' A$
    $= A'Bx + AB'x = (A \oplus B)\, x$
  - $B(t+1) = B'x$

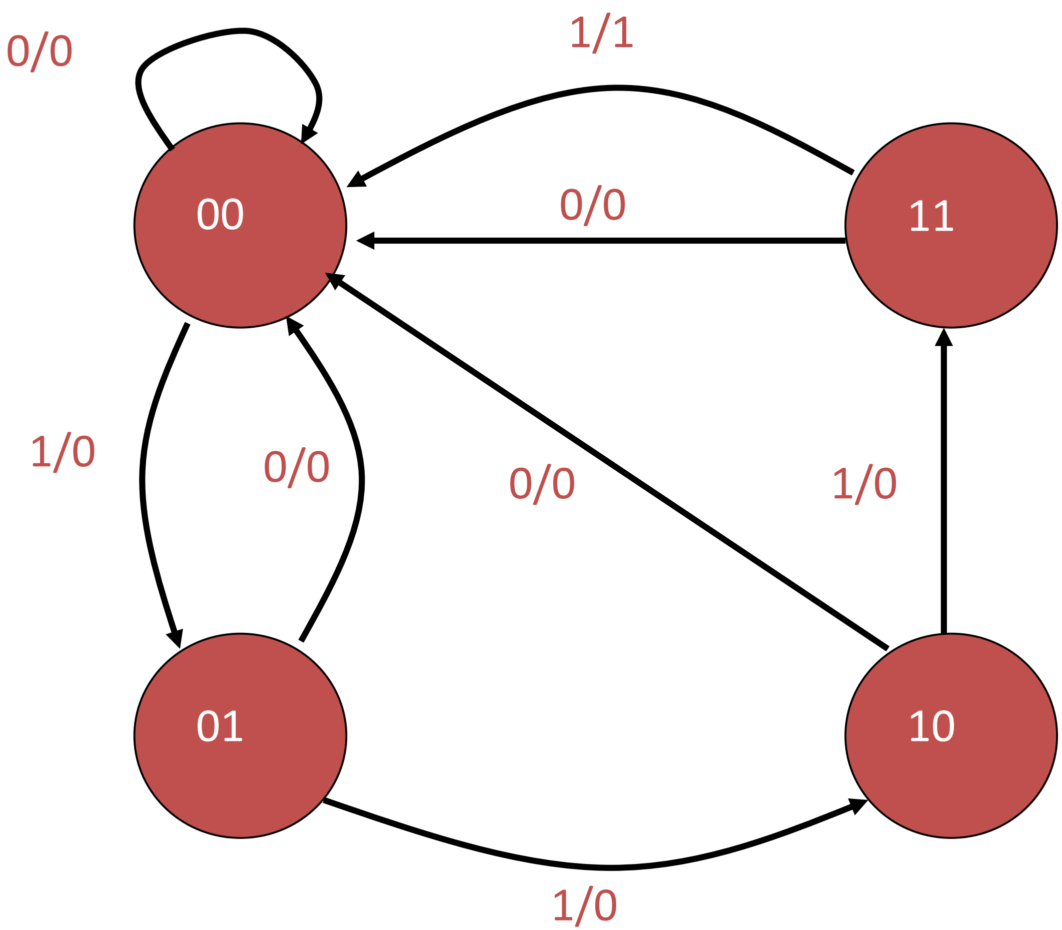
State Diagram



Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

What is the circuit doing?

State Diagram



Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

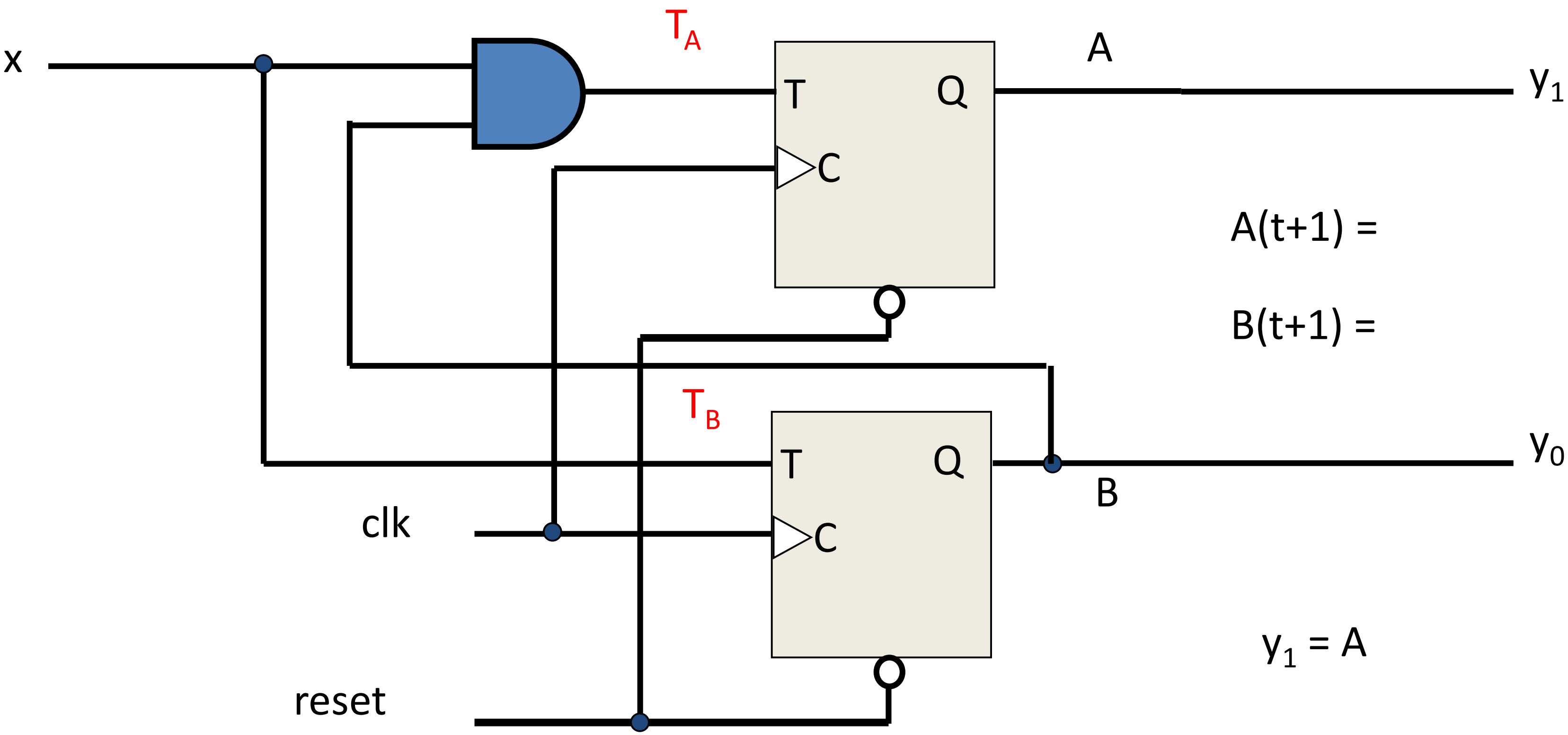
What is the circuit doing?

Analysis with T Flip-Flops

- Method is the same
- Example

$T_A =$

$T_B =$



$A(t+1) =$

$B(t+1) =$

$y_1 = A$

$y_0 = B$

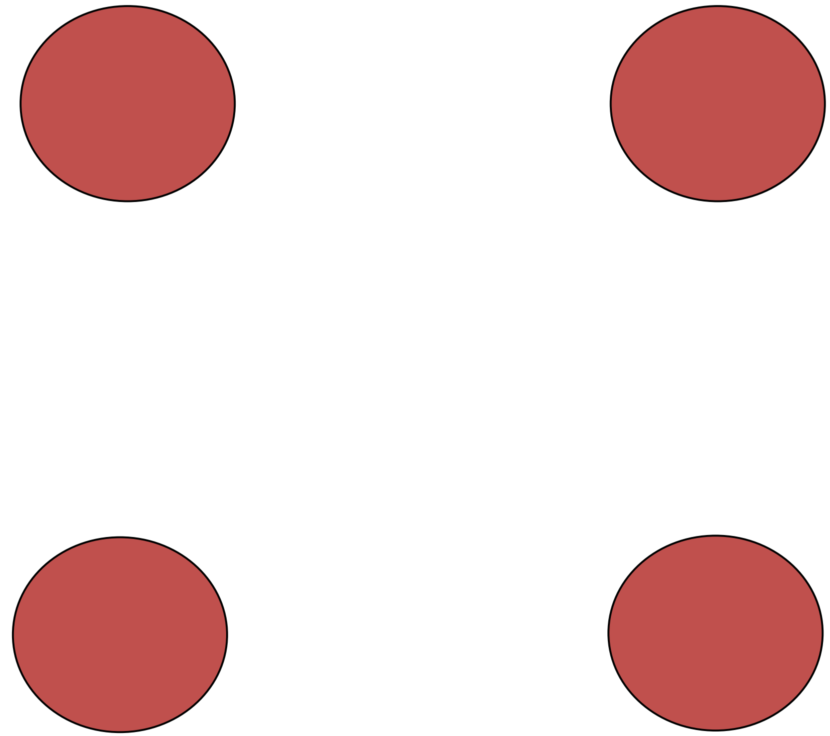
Example: Analysis with T Flip-Flops

- Characteristic equation
  - $A(t+1) = T_A \oplus A$
  - $B(t+1) = T_B \oplus B$
- Input equations
  - $T_A = Bx$
  - $T_B = x$
- Output equations
  - $y_1 = A$
  - $y_0 = B$
- State equations
  - $A(t+1) =$
  - $B(t+1) =$

State Table & Diagram

- $A(t+1) = xB \oplus A$
- $B(t+1) = x \oplus B$
- $y_1 = A$; $y_0 = B$

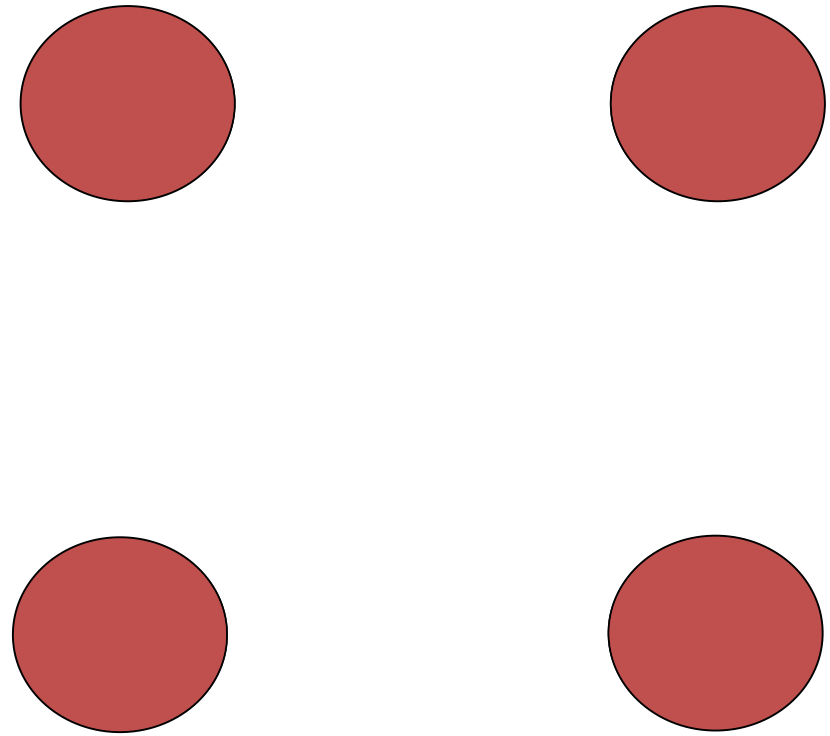
Present state		input	Next state		output	
A	B	x	A	B	y_1	y_0
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				



State Table & Diagram

- $A(t+1) = xB \oplus A$
- $B(t+1) = x \oplus B$
- $y_1 = A$; $y_0 = B$

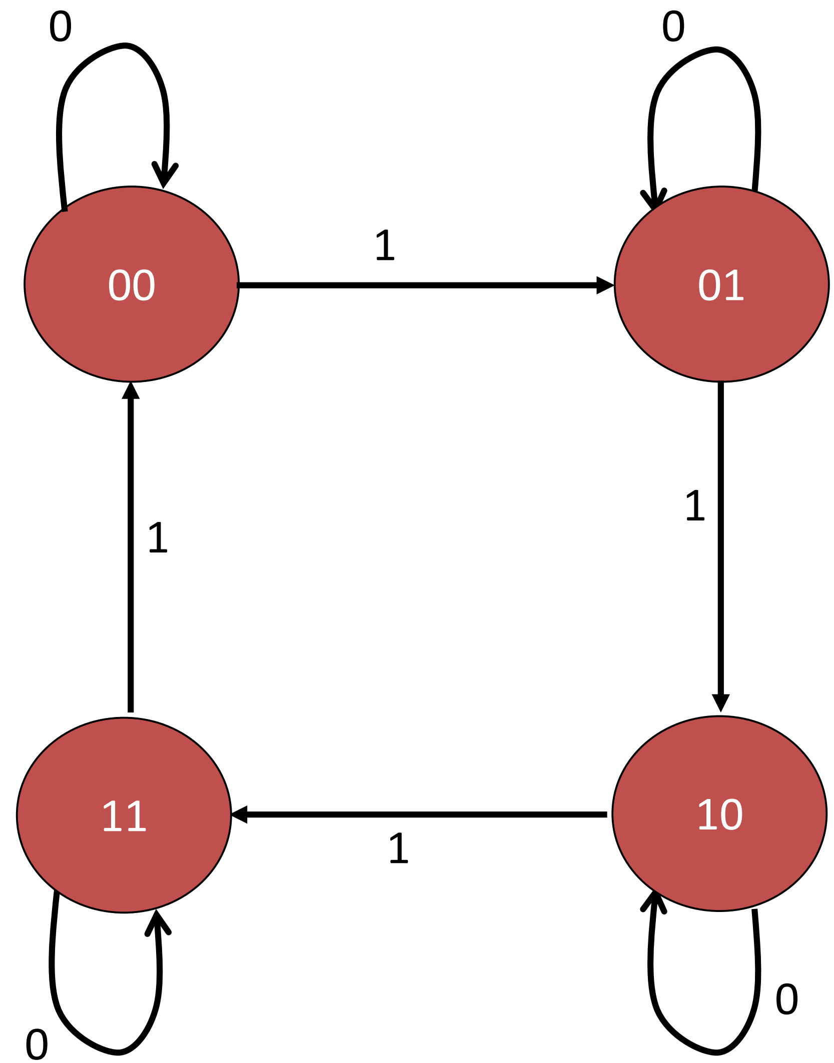
Present state		input	Next state		output	
A	B	x	A	B	y_1	y_0
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	1	1	0
1	1	0	1	1	1	1
1	1	1	0	0	1	1



State Table & Diagram

- $A(t+1) = xB \oplus A$
- $B(t+1) = x \oplus B$
- $y_1 = A$; $y_0 = B$

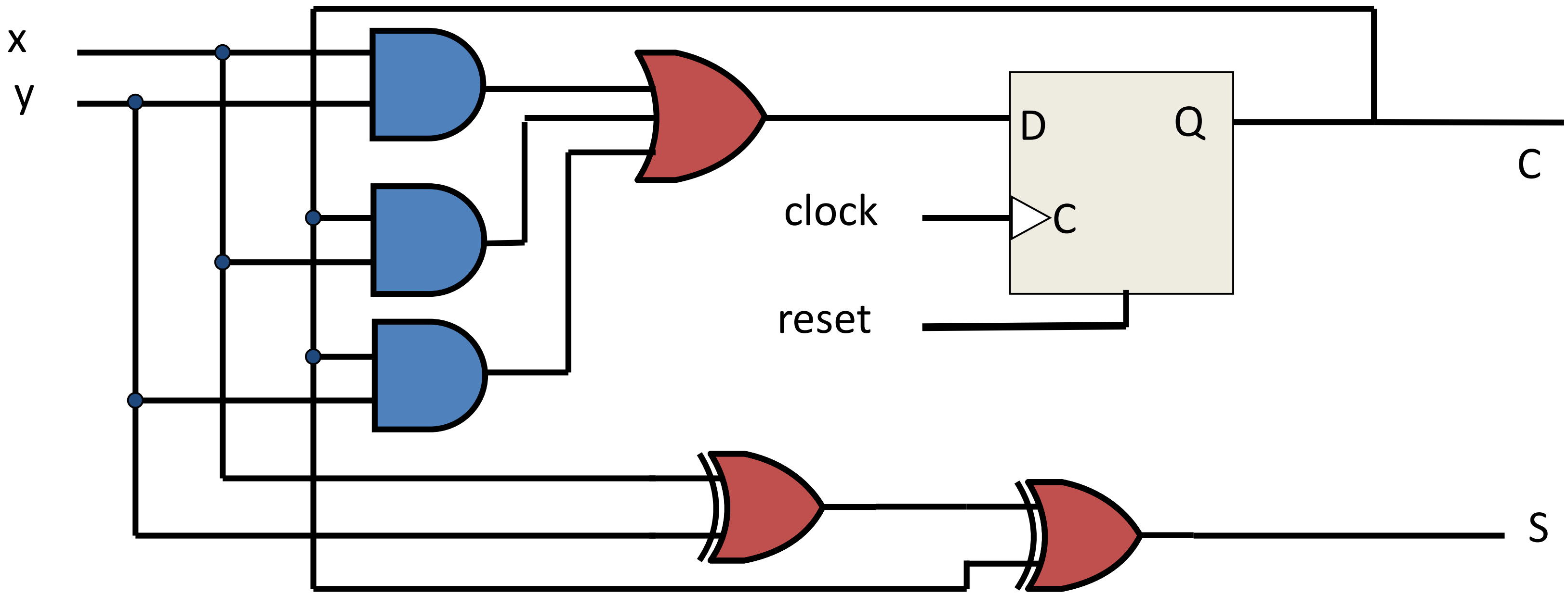
Present state A	Present state B	input x	Next state A	Next state B	output y_1	output y_0
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	1	1	0
1	1	0	1	1	1	1
1	1	1	0	0	1	1



Mealy and Moore Models

- There are two models for sequential circuits
  - Mealy
  - Moore
- They differ in the way the outputs are generated
  - Mealy:
    - output is a function of **both present states and inputs**
  - Moore
    - output is a function of **present state only**

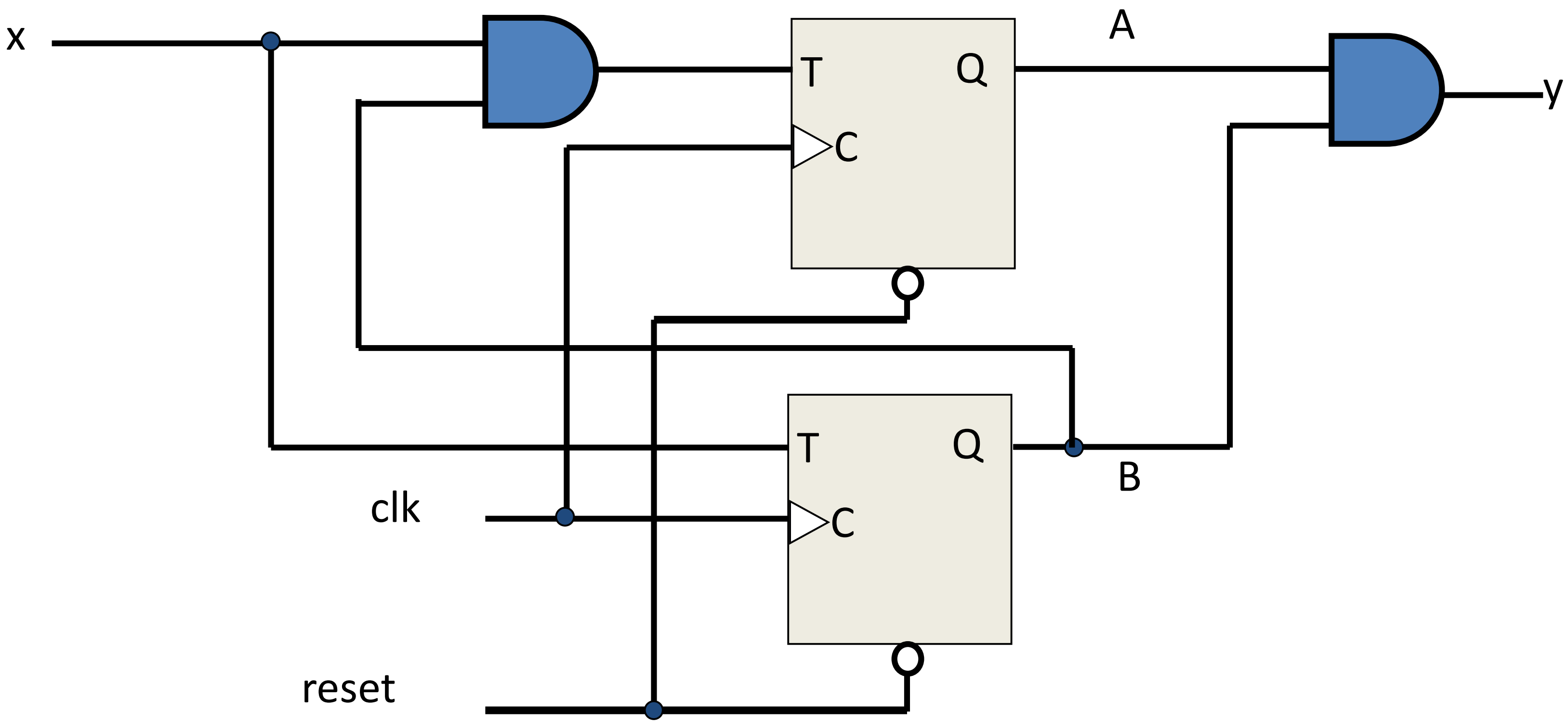
Example: Mealy and Moore Machines



a Mealy machine

- External inputs x and y are asynchronous
- Thus, outputs may have momentary (incorrect) values
- Inputs must be synchronized with clocks
- Outputs must be sampled only during clock edges

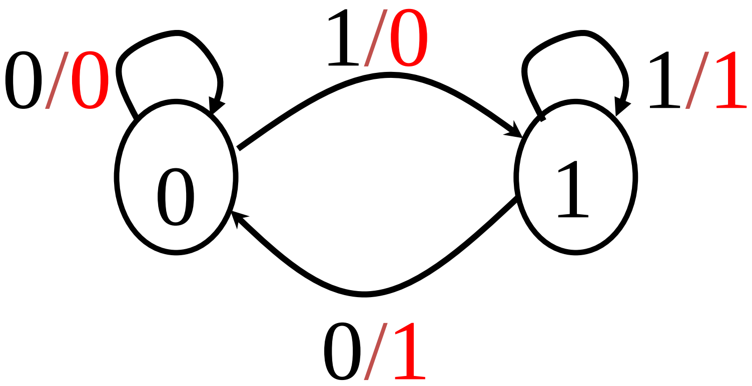
Example: Moore Machines



- Outputs are already synchronized with clock.
- They change synchronously with the clock edge.

Design Example - 1

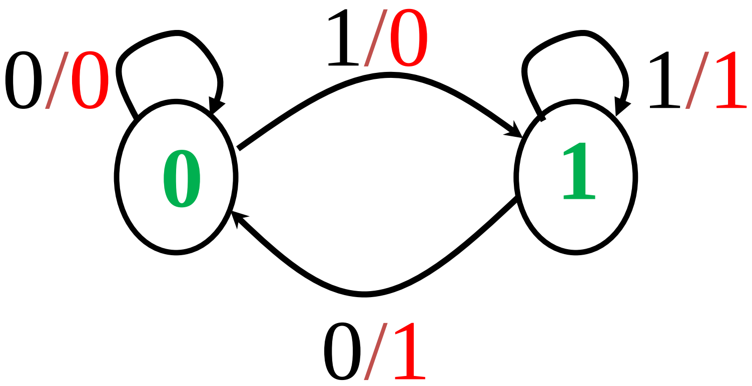
- Implement the following state diagram with D FFs.



x	Q(t)	Q(t+1)	D	Z

Design Example - 1

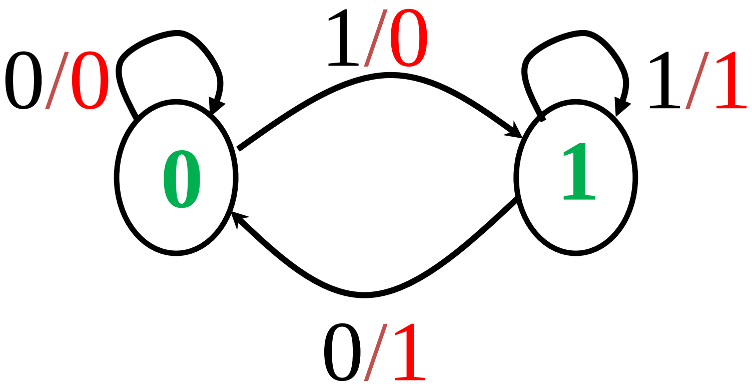
- Implement the following state diagram with D FFs.



x	Q(t)	Q(t+1)	D	Z
0	0			
0	1			
1	0			
1	1			

Design Example - 1

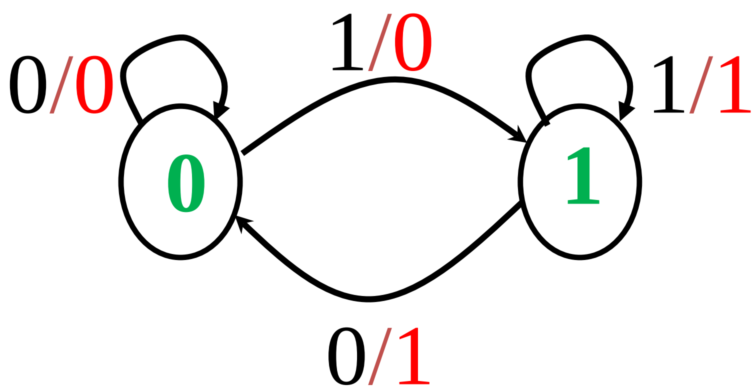
- Implement the following state diagram with D FFs.



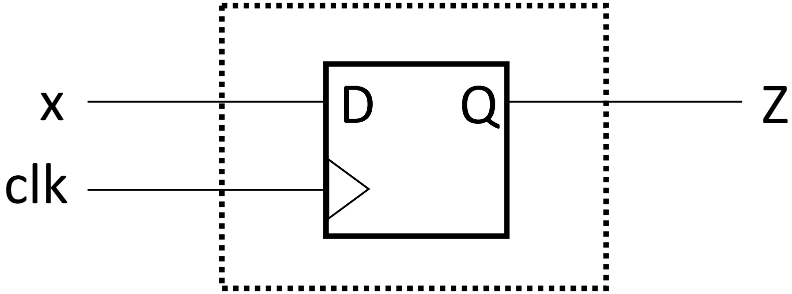
x	Q(t)	Q(t+1)	D	Z
0	0	0		0
0	1	0		1
1	0	1		0
1	1	1		1

Design Example - 1

- Implement the following state diagram with D FFs.



x	Q(t)	Q(t+1)	D	Z
0	0	0	0	0
0	1	0	0	1
1	0	1	1	0
1	1	1	1	1

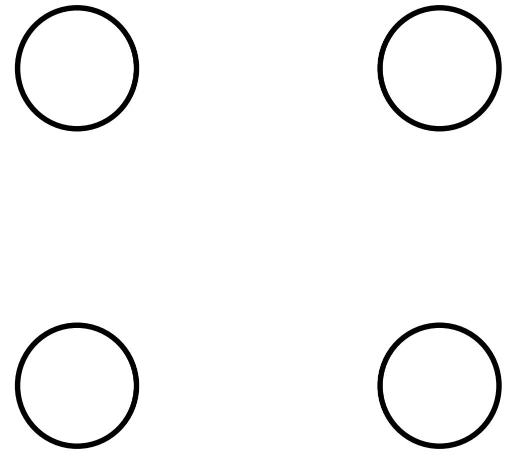


Design Example - 2

- Design a sequential circuit that counts up (00, 01, 10, 11, 00,…) when x=1, and counts down (00,11,10,01,00,…) when x=0. Use JK FFs.

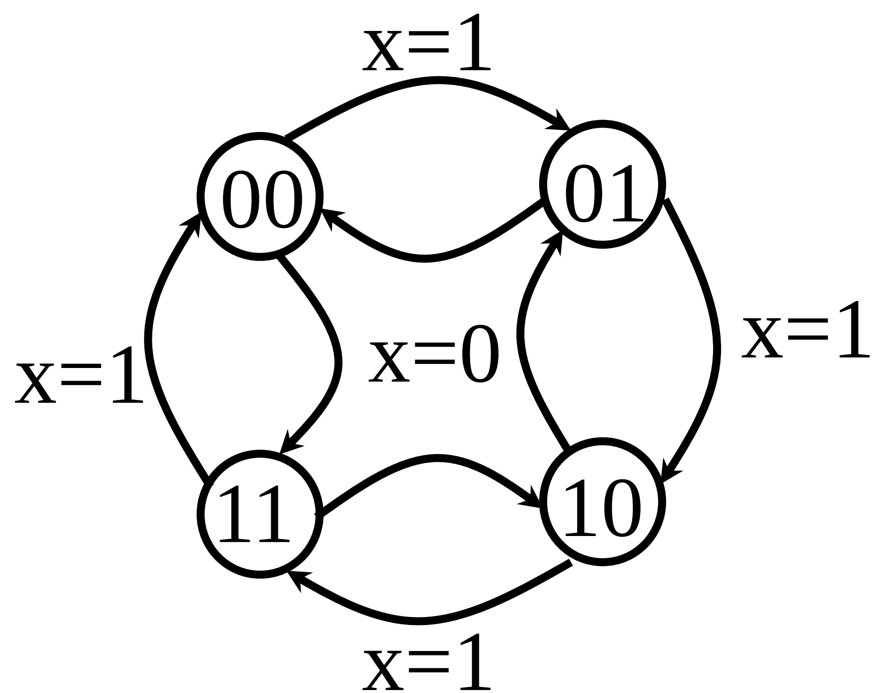
Design Example - 2

- Design a sequential circuit
  - that counts up (00, 01, 10, 11,00,…) when x=1,
  - and counts down (00,11,10,01,00,…) when x=0. Use JK FFs.



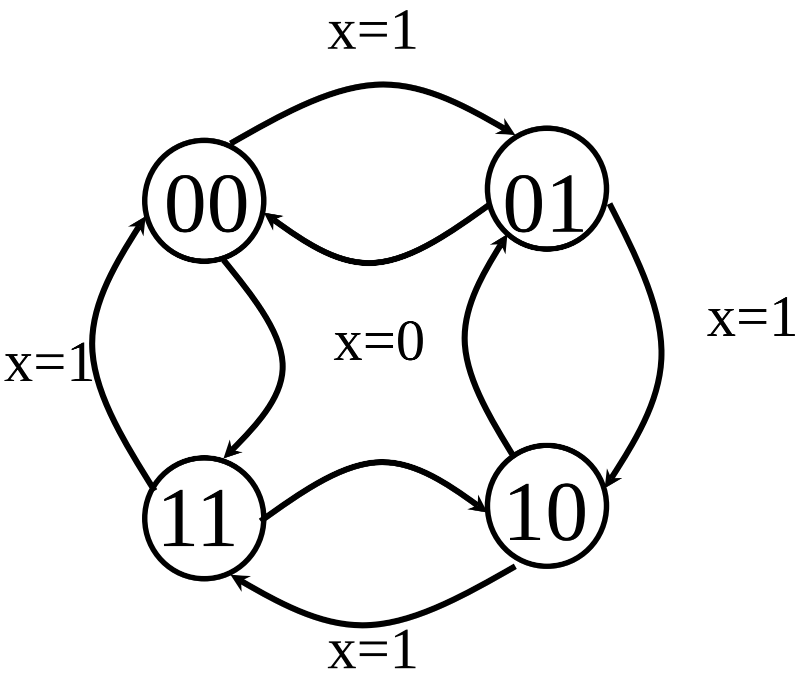
Design Example - 2

- Design a sequential circuit
  - that counts up (00, 01, 10, 11,00,…) when x=1,
  - and counts down (00,11,10,01,00,…) when x=0. Use JK FFs.



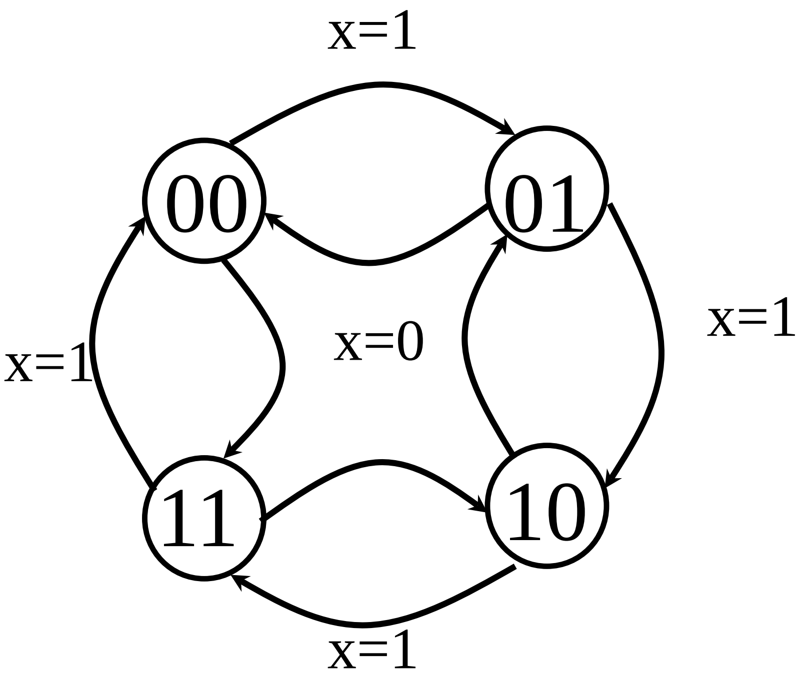
Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B



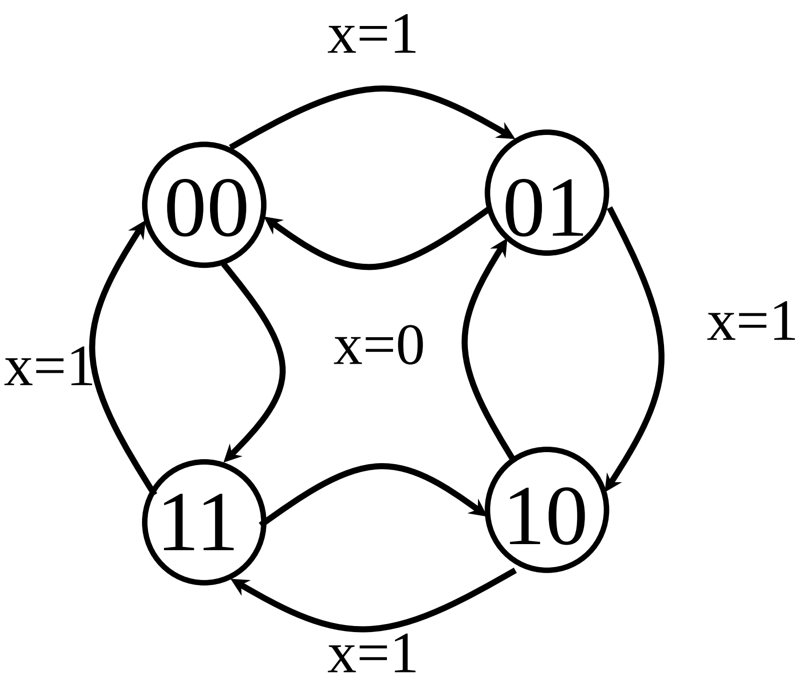
Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						



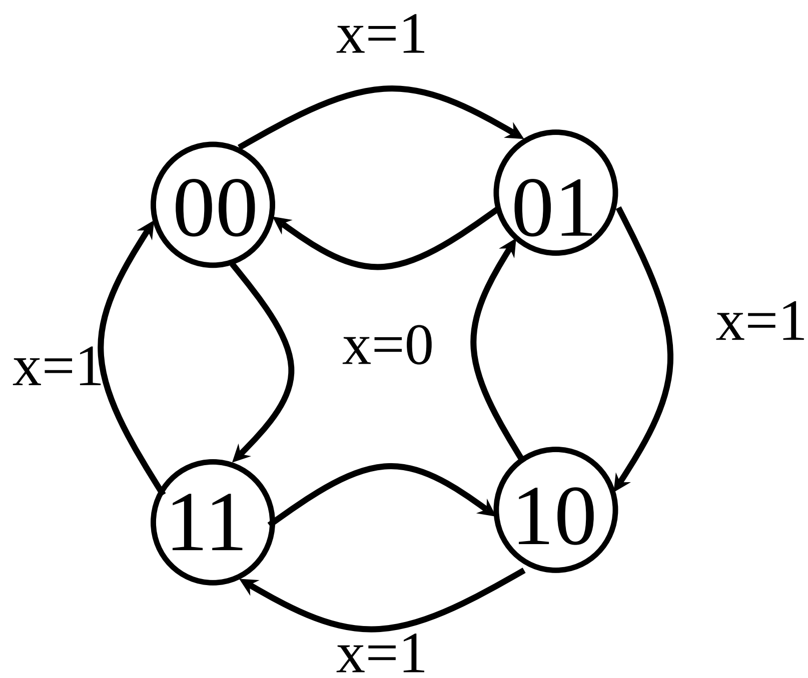
Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1				
0	0	1	0	0				
0	1	0	0	1				
0	1	1	1	0				
1	0	0	0	1				
1	0	1	1	0				
1	1	0	1	1				
1	1	1	0	0				



Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1				
0	0	1	0	0				
0	1	0	0	1				
0	1	1	1	0				
1	0	0	0	1				
1	0	1	1	0				
1	1	0	1	1				
1	1	1	0	0				

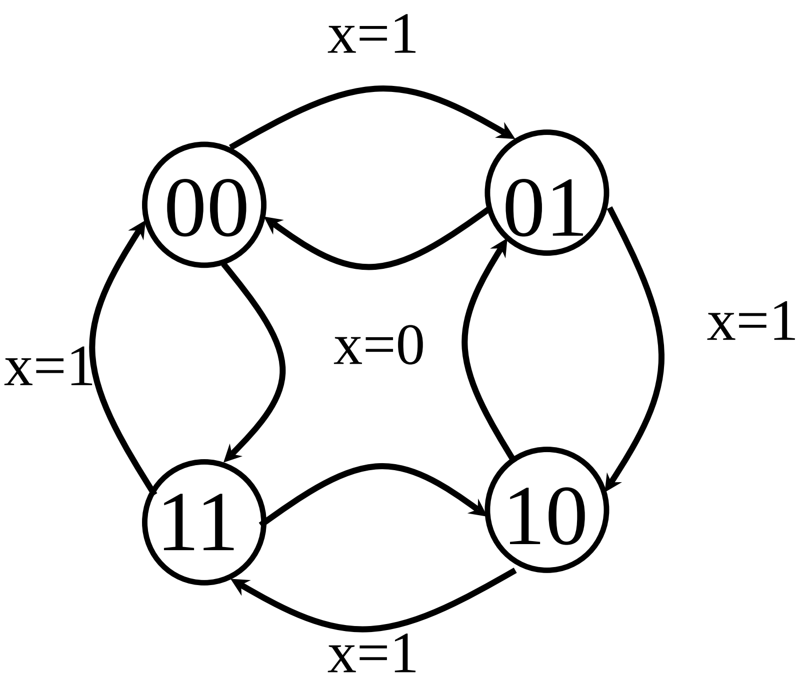


$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1			
0	0	1	0	0	0			
0	1	0	0	1	X			
0	1	1	1	0	X			
1	0	0	0	1	0			
1	0	1	1	0	1			
1	1	0	1	1	X			
1	1	1	0	0	X			

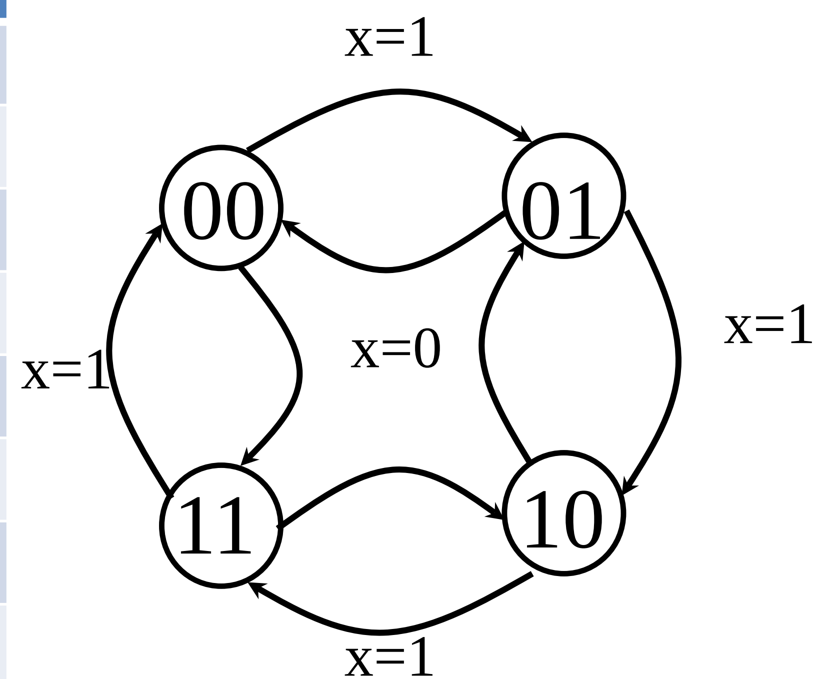


$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X		
0	0	1	0	0	0	X		
0	1	0	0	1	X	1		
0	1	1	1	0	X	0		
1	0	0	0	1	0	X		
1	0	1	1	0	1	X		
1	1	0	1	1	X	0		
1	1	1	0	0	X	1		

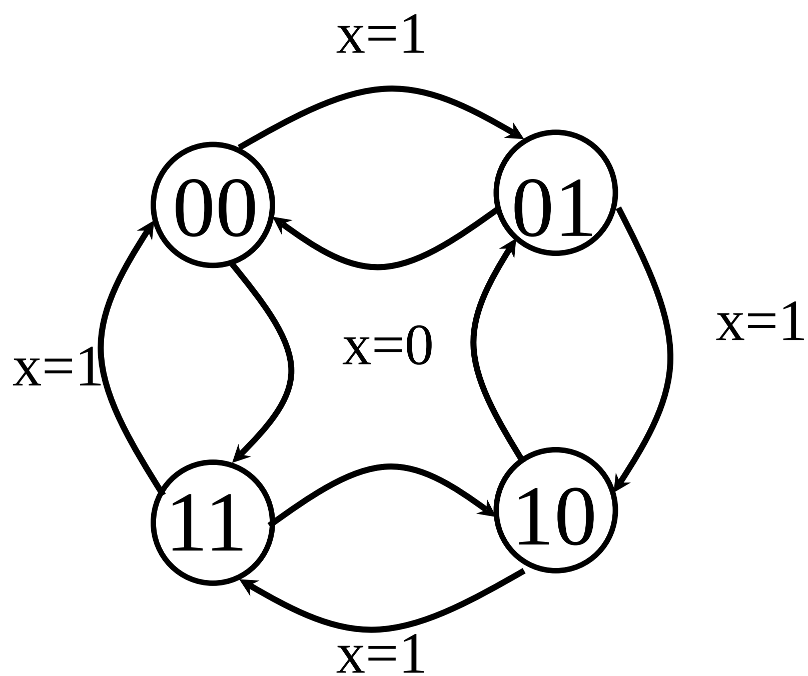


$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	
0	0	1	0	0	0	X	X	
0	1	0	0	1	X	1	1	
0	1	1	1	0	X	0	X	
1	0	0	0	1	0	X	1	
1	0	1	1	0	1	X	X	
1	1	0	1	1	X	0	1	
1	1	1	0	0	X	1	X	

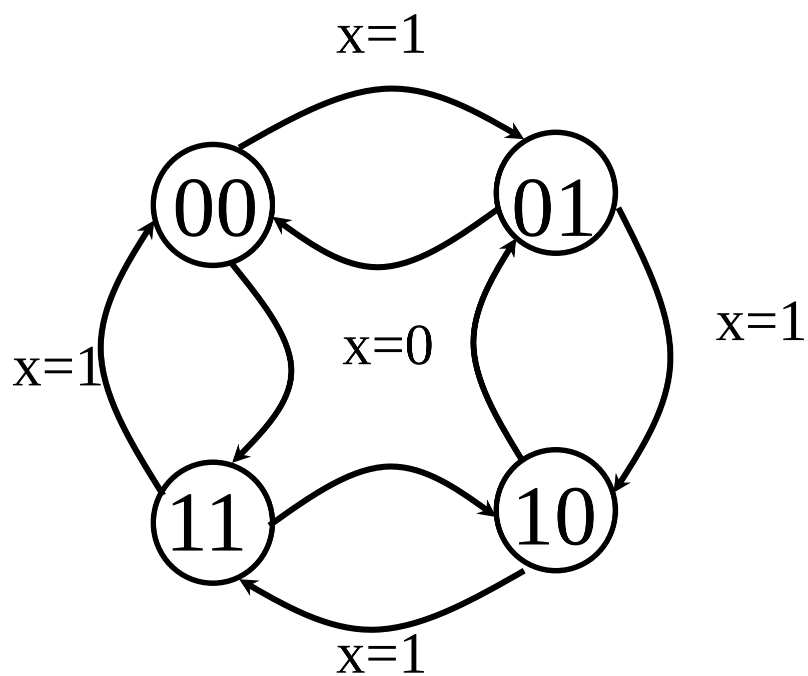


$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
0	0	1	0	0	0	X	X	1
0	1	0	0	1	X	1	1	X
0	1	1	1	0	X	0	X	1
1	0	0	0	1	0	X	1	X
1	0	1	1	0	1	X	X	1
1	1	0	1	1	X	0	1	X
1	1	1	0	0	X	1	X	1

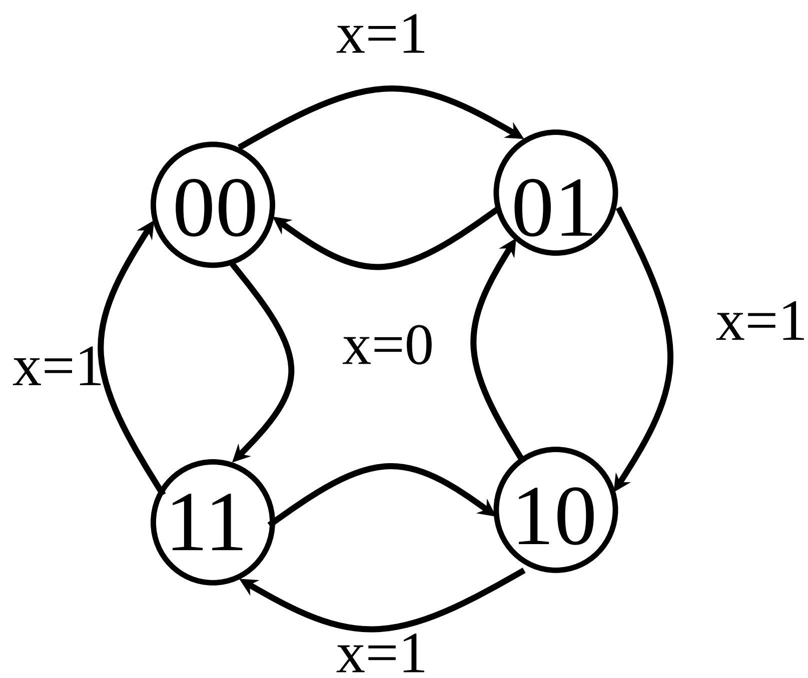


$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases}$$

$$K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
0	0	1	0	0	0	X	X	1
0	1	0	0	1	X	1	1	X
0	1	1	1	0	X	0	X	1
1	0	0	0	1	0	X	1	X
1	0	1	1	0	1	X	X	1
1	1	0	1	1	X	0	1	X
1	1	1	0	0	X	1	X	1



$J_A =$?

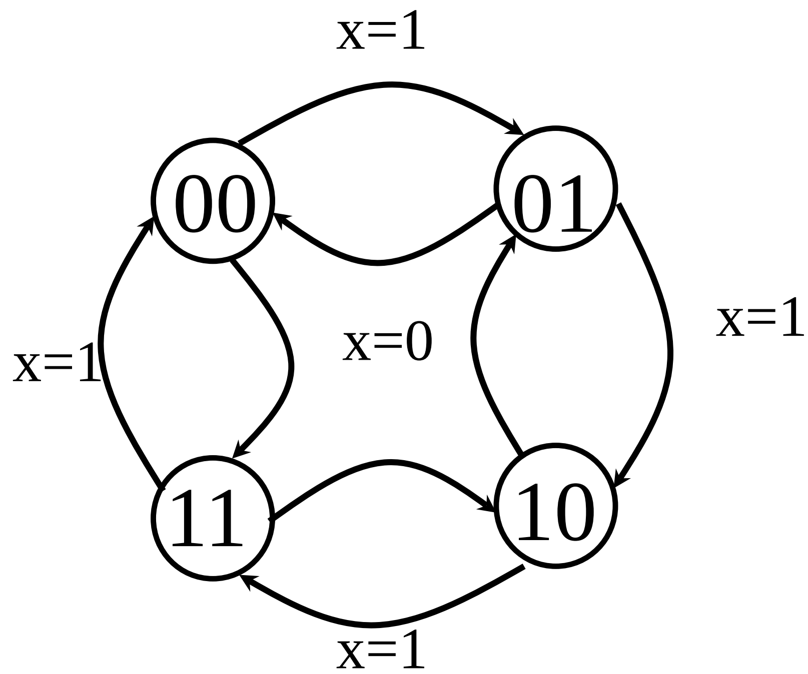
$J_B =$?

$K_A =$?

$K_B =$?

Design Example - 2

x	A	B	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
0	0	1	0	0	0	X	X	1
0	1	0	0	1	X	1	1	X
0	1	1	1	0	X	0	X	1
1	0	0	0	1	0	X	1	X
1	0	1	1	0	1	X	X	1
1	1	0	1	1	X	0	1	X
1	1	1	0	0	X	1	X	1



x \ AB	00	01	11	10
0	1	0	X	X
1	0	1	X	X

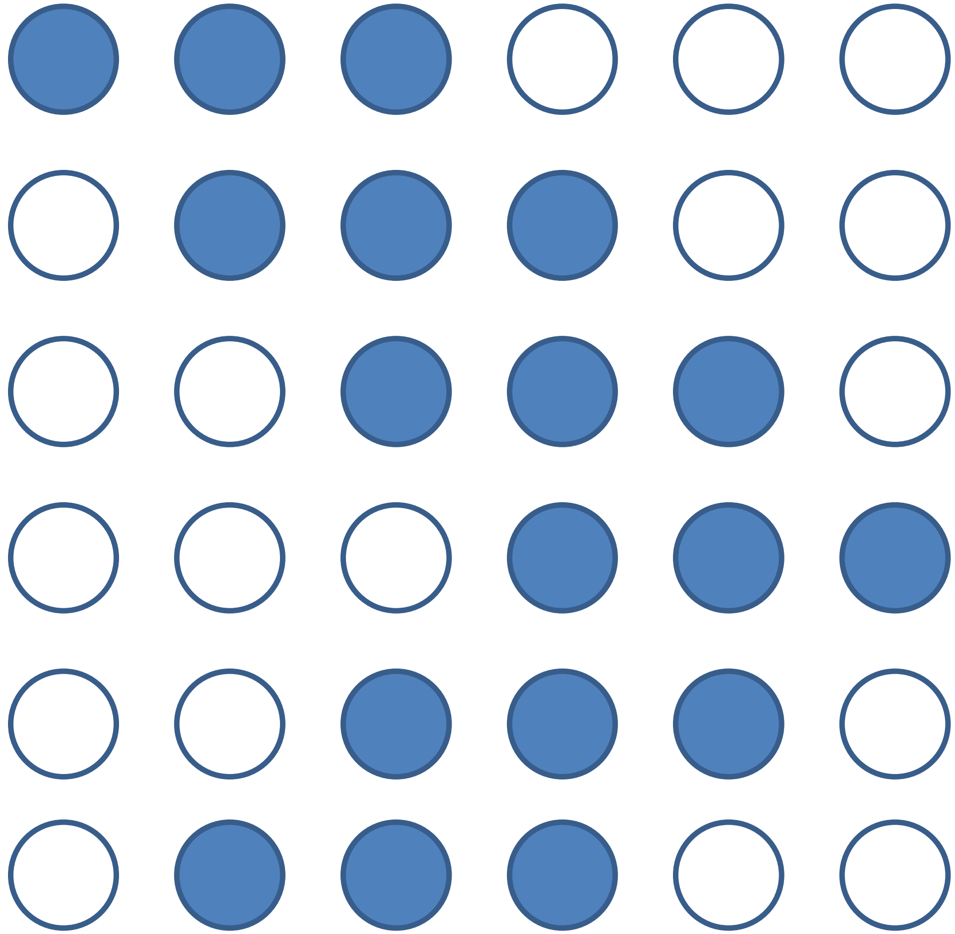
x \ AB	00	01	11	10
0	X	X	0	1
1	X	X	1	0

Design Example - 2

- $J_A = xB+x'B'$
- $K_A = xB+x'B'$
- $J_B=1$
- $K_B=1$
- **Let’s draw the circuit**

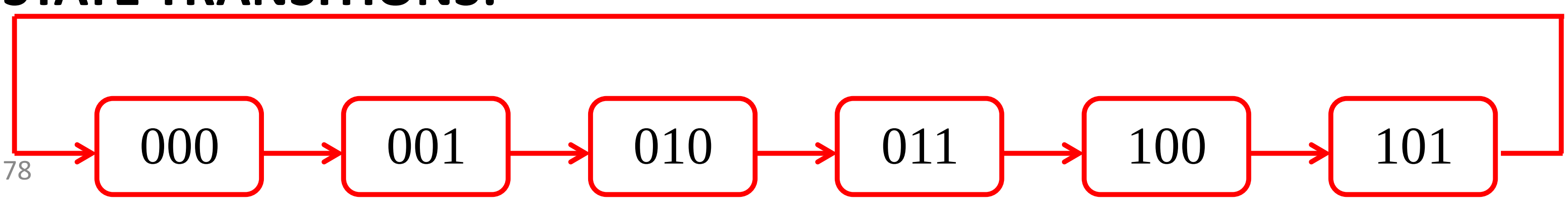
Design Example - 3

OUTPUTS:



design with JK flip-flops

STATE TRANSITIONS:

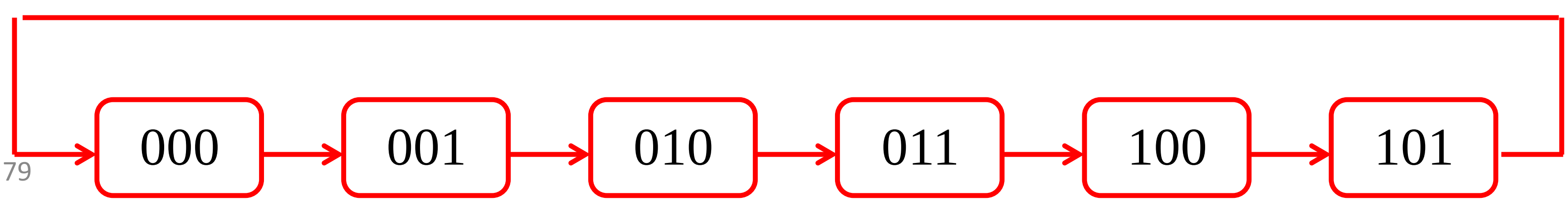


Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
						1	1	1	0	0	0						
						0	1	1	1	0	0						
						0	0	1	1	1	0						
						0	0	0	1	1	1						
						0	0	1	1	1	0						
						0	1	1	1	0	0						

$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$

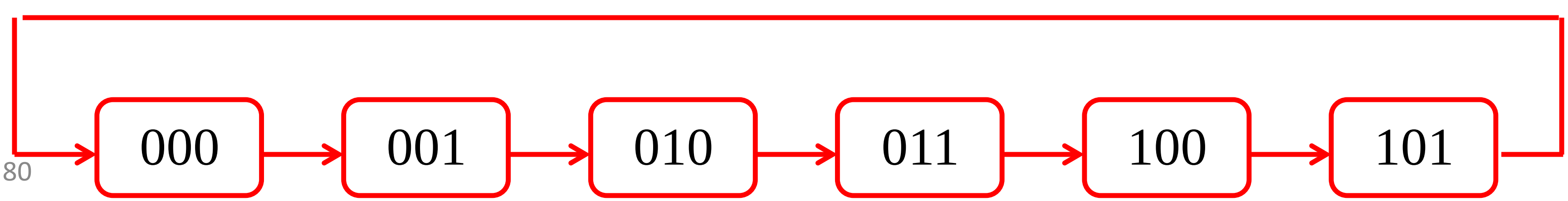
Mealy or Moore?



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	1	1	1	0	0	0						
0	0	1	0	1	0	0	1	1	1	0	0						
0	1	0	0	1	1	0	0	1	1	1	0						
0	1	1	1	0	0	0	0	0	1	1	1						
1	0	0	1	0	1	0	0	1	1	1	0						
1	0	1	0	0	0	0	1	1	1	0	0						

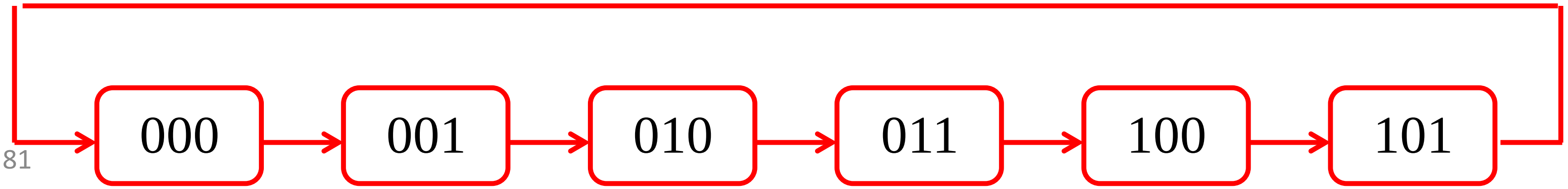
$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	1	1	1	0	0	0	0		0		1	
0	0	1	0	1	0	0	1	1	1	0	0	0		1			
0	1	0	0	1	1	0	0	1	1	1	0	0				1	
0	1	1	1	0	0	0	0	0	1	1	1	1					
1	0	0	1	0	1	0	0	1	1	1	0			0		1	
1	0	1	0	0	0	0	1	1	1	0	0			0			

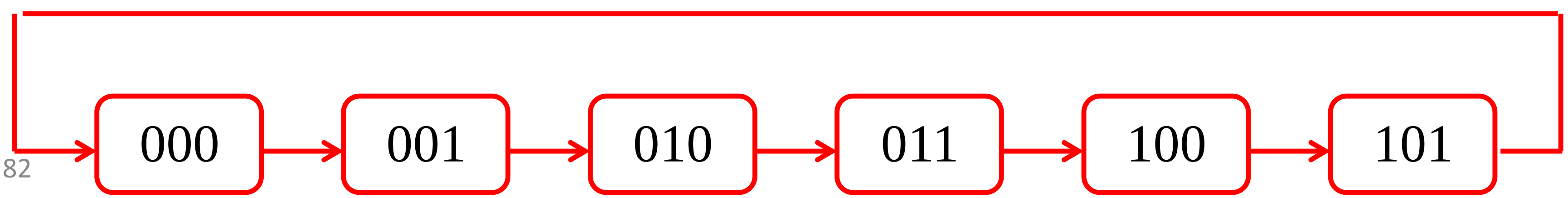
$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	1	1	1	0	0	0	0		0		1	
0	0	1	0	1	0	0	1	1	1	0	0	0		1		X	
0	1	0	0	1	1	0	0	1	1	1	0	0		X		1	
0	1	1	1	0	0	0	0	0	1	1	1	1		X		X	
1	0	0	1	0	1	0	0	1	1	1	0	X		0		1	
1	0	1	0	0	0	0	1	1	1	0	0	X		0		X	

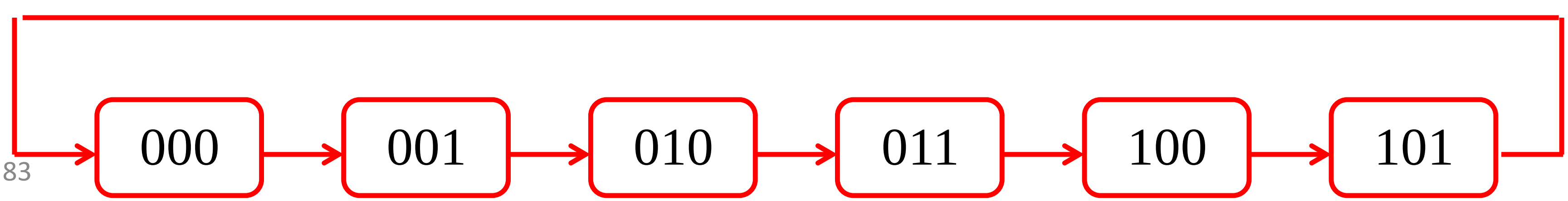
$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	1	1	1	0	0	0	0		0		1	
0	0	1	0	1	0	0	1	1	1	0	0	0		1		X	1
0	1	0	0	1	1	0	0	1	1	1	0	0		X	0	1	
0	1	1	1	0	0	0	0	0	1	1	1	1		X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0		1	
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0		X	1

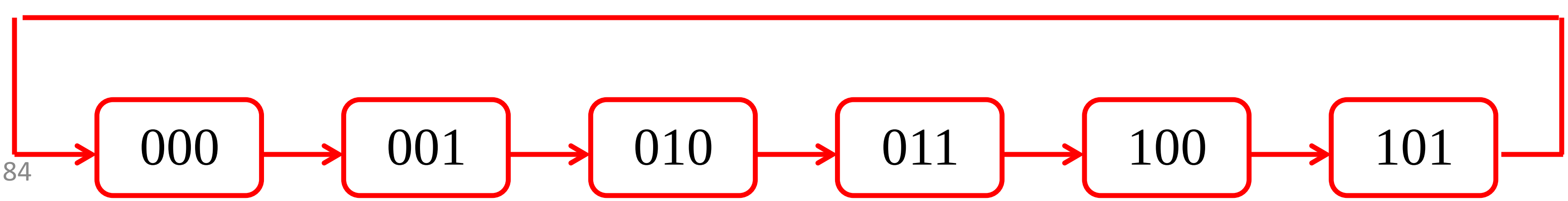
$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1

$$J = \begin{cases} Q(t+1) & Q(t)=0 \\ X & Q(t)=1 \end{cases} \qquad K = \begin{cases} Q(t+1)' & Q(t)=1 \\ X & Q(t)=0 \end{cases}$$



Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

A \ BC	00	01	11	10
0	0	0	1	0
1	X	X	X	X

J_A=

A \ BC	00	01	11	10
0	X	X	X	X
1	0	1	X	X

K_A=

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

A \ BC	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_A = BC$

A \ BC	00	01	11	10
0	X	X	X	X
1	0	1	X	X

$K_A = C$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

A \ BC	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_B =$

A \ BC	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$K_B =$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

A \ BC	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_B = A'C$

A \ BC	00	01	11	10
0	X	X	1	0
1	X	X	X	X

$K_B = C$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

A \ BC	00	01	11	10
0	1	X	1	X
1	1	X	X	X

$J_C=$

A \ BC	00	01	11	10
0	X	1	1	X
1	X	1	X	X

$K_C=$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	X	0	X	1	X
0	0	1	0	1	0	0	1	1	1	0	0	0	X	1	X	X	1
0	1	0	0	1	1	0	0	1	1	1	0	0	X	X	0	1	X
0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	1	X	1
1	0	0	1	0	1	0	0	1	1	1	0	X	0	0	X	1	X
1	0	1	0	0	0	0	1	1	1	0	0	X	1	0	X	X	1
1	1	0										X	X	X	X	X	X
1	1	1										X	X	X	X	X	X

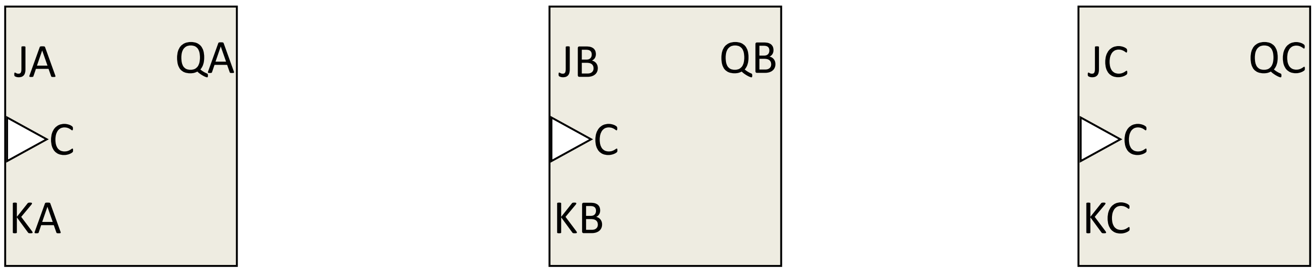
A \ BC	00	01	11	10
0	1	X	1	X
1	1	X	X	X

$J_C=1$

A \ BC	00	01	11	10
0	X	1	1	X
1	X	1	X	X

$K_C=1$

Design Example - 3



We can also solve for outputs z1-z6 by looking at K-maps of A(t),B(t),C(t)

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	1	0	0	0	1	1	1	1	1
0	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	1	1
1	0	1	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1
1	1	0															
1	1	1															

$J_A = BC$

$K_A = C$

$J_B = A'C$

$K_B = C$

$J_C = 1$

$K_C = 1$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	1	0	0	0	1	1	1	1	1
0	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	1	1
1	0	1	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1
1	1	0										0	0	0	0	1	1
1	1	1										1	1	0	1	1	1

$J_A = BC$

$K_A = C$

$J_B = A'C$

$K_B = C$

$J_C = 1$

$K_C = 1$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	1	0	0	0	1	1	1	1	1
0	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	1	1
1	0	1	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1
1	1	0	1	1	1							0	0	0	0	1	1
1	1	1	0	0	0							1	1	0	1	1	1

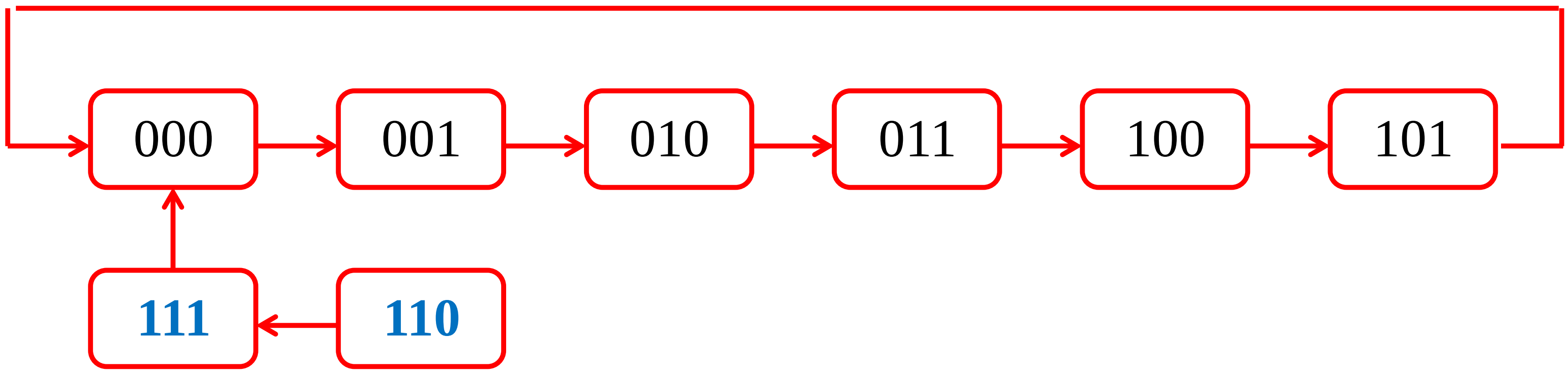
$J_A=BC$ $\quad$ $A(t+1)=BCA'+C'A$ $\quad$ $K_A=C$

$J_B=A'C$ $\quad$ $B(t+1)=A'CB'+C'B$ $\quad$ $K_B=C$

$J_C=1$ $\quad$ $C(t+1)=C'$ $\quad$ $K_C=1$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	1	0	0	0	1	1	1	1	1
0	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	1	1
1	0	1	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1
1	1	0	1	1	1							0	0	0	0	1	1
1	1	1	0	0	0							1	1	0	1	1	1



Design Example - 3

- now let’s redo the design with D FFs

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	DA	DB	DC
0	0	0	0	0	1	1	1	1	0	0	0			
0	0	1	0	1	0	0	1	1	1	0	0			
0	1	0	0	1	1	0	0	1	1	1	0			
0	1	1	1	0	0	0	0	0	1	1	1			
1	0	0	1	0	1	0	0	1	1	1	0			
1	0	1	0	0	0	0	1	1	1	0	0			
1	1	0	1	1	1									
1	1	1	0	0	0									

$A(t+1)=BCA'+C'A\ =$

$B(t+1)=A'CB'+C'B\ =$

$C(t+1)=C'\ =$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	DA	DB	DC
0	0	0	0	0	1	1	1	1	0	0	0			
0	0	1	0	1	0	0	1	1	1	0	0			
0	1	0	0	1	1	0	0	1	1	1	0			
0	1	1	1	0	0	0	0	0	1	1	1			
1	0	0	1	0	1	0	0	1	1	1	0			
1	0	1	0	0	0	0	1	1	1	0	0			
1	1	0	1	1	1									
1	1	1	0	0	0									

$A(t+1)=BCA'+C'A = D_A$

$B(t+1)=A'CB'+C'B = D_B$

$C(t+1)=C' = D_C$

Design Example - 3

A(t)	B(t)	C(t)	A (t+1)	B (t+1)	C (t+1)	z1	z2	z3	z4	z5	z6	DA	DB	DC
0	0	0	0	0	1	1	1	1	0	0	0			1
0	0	1	0	1	0	0	1	1	1	0	0		1	
0	1	0	0	1	1	0	0	1	1	1	0		1	1
0	1	1	1	0	0	0	0	0	1	1	1	1		
1	0	0	1	0	1	0	0	1	1	1	0	1		1
1	0	1	0	0	0	0	1	1	1	0	0			
1	1	0	1	1	1							1	1	1
1	1	1	0	0	0									

$A(t+1) = BCA' + C'A = D_A$

$B(t+1) = A'CB' + C'B = D_B$

$C(t+1) = C' = D_C$

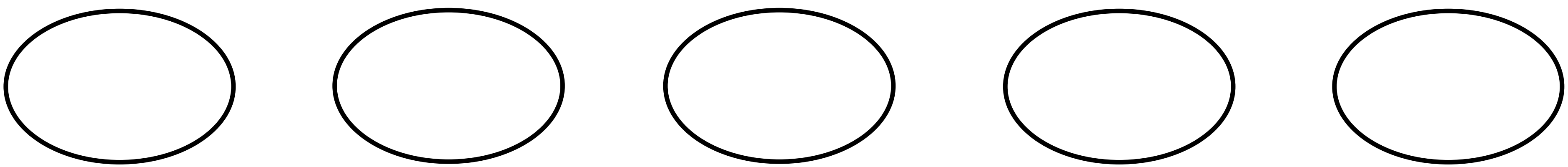
Design Example - 4

- Design a logic circuit with JK flip-flops that detects the sequence 1011 and outputs 1 in that case, 0 otherwise.

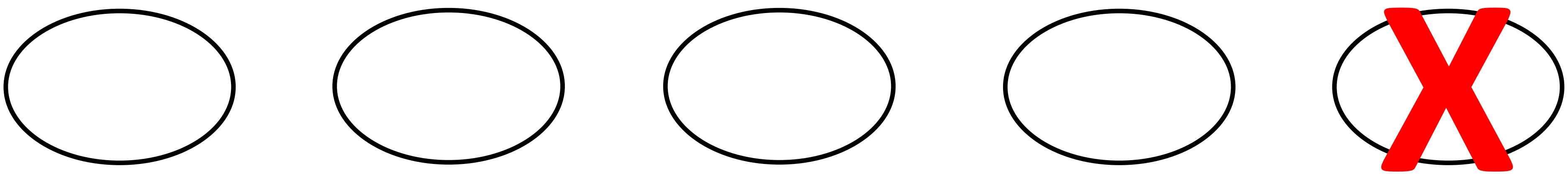
Design Example - 4

?

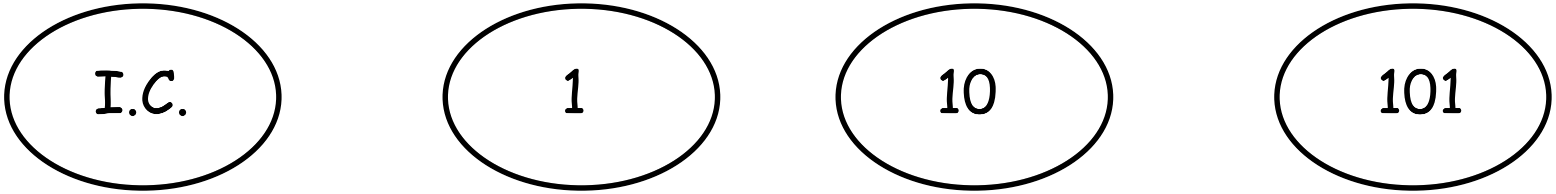
Design Example - 4



Design Example - 4



Design Example - 4

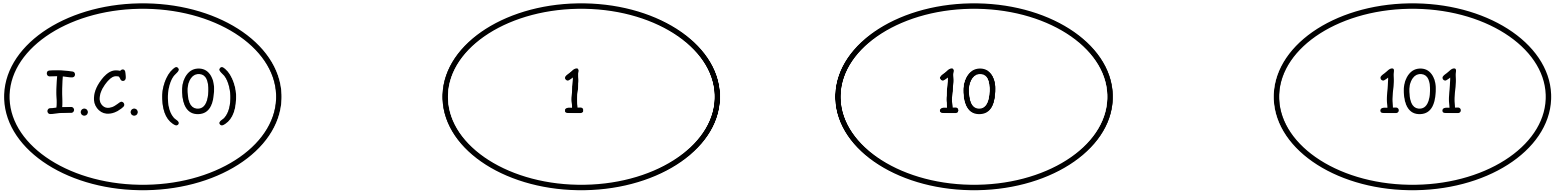


Design Example - 4

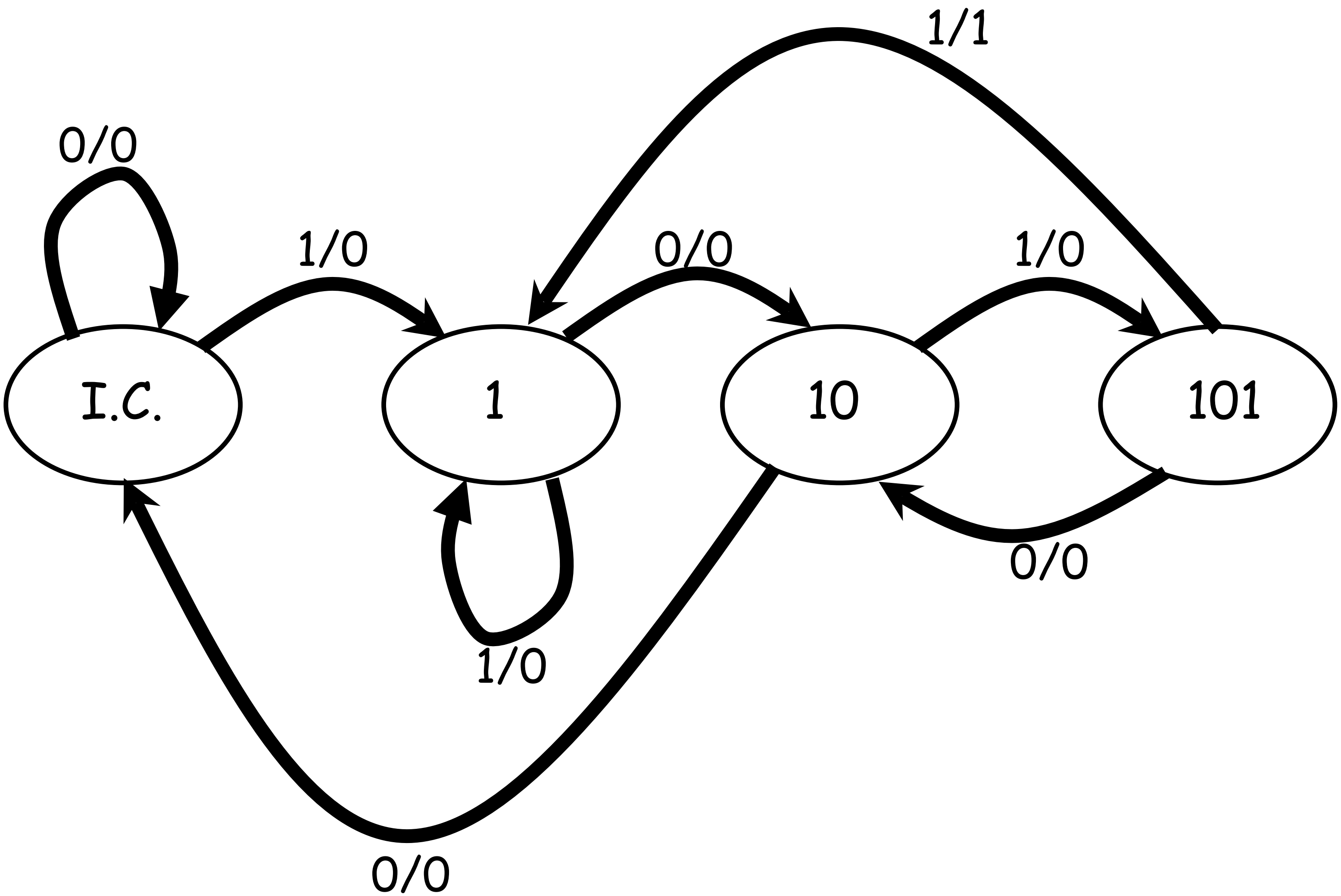
consider the sequence:

00100101011011001

consider the sequence:
00100101011011001

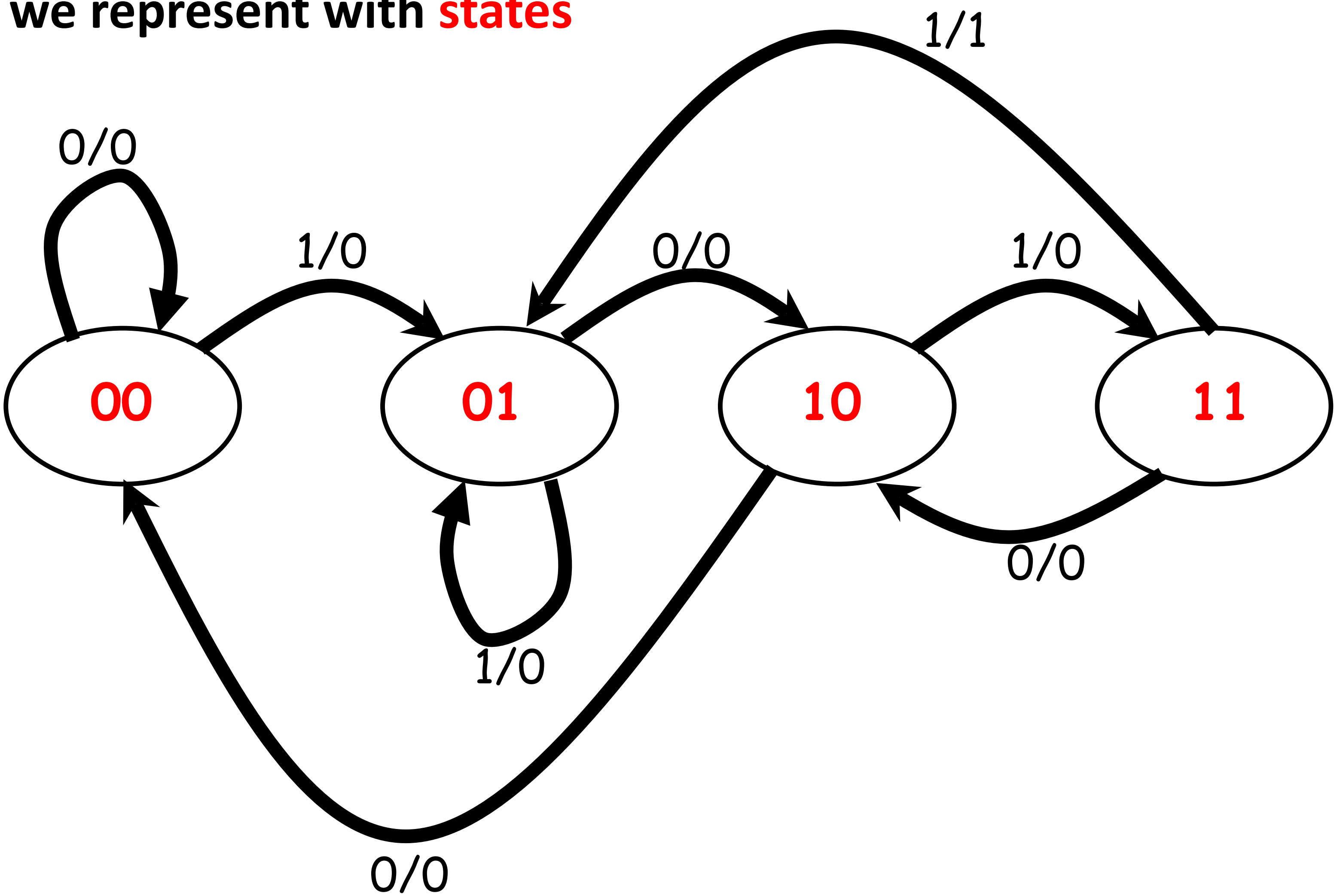


Design Example - 4



Design Example - 4

now we represent with states



Design Example - 4

x(t)	A(t)	B(t)	A (t+1)	B (t+1)	Z	J_A	K_A	J_B	K_B

Design Example - 4

x(t)	A(t)	B(t)	A (t+1)	B (t+1)	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0				
0	0	1	1	0	0				
0	1	0	0	0	0				
0	1	1	1	0	0				
1	0	0	0	1	0				
1	0	1	0	1	0				
1	1	0	1	1	0				
1	1	1	0	1	1				

Design Example - 4

x(t)	A(t)	B(t)	A (t+1)	B (t+1)	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	1	0	0	1	X	X	1
0	1	0	0	0	0	X	1	0	X
0	1	1	1	0	0	X	0	X	1
1	0	0	0	1	0	0	X	1	X
1	0	1	0	1	0	0	X	X	0
1	1	0	1	1	0	X	0	1	X
1	1	1	0	1	1	X	1	X	0

Design Example - 4

x \ AB	00	01	11	10
0				
1				

$J_A=$

x \ AB	00	01	11	10
0				
1				

$K_A=$

x \ AB	00	01	11	10
0				
1				

$J_B=$

x \ AB	00	01	11	10
0				
1				

$K_B=$

Design Example - 4

x \ AB	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_A = x'B$

x \ AB	00	01	11	10
0	X	X	0	1
1	X	X	1	0

$K_A = xB + x'B'$

x \ AB	00	01	11	10
0	0	X	X	0
1	1	X	X	1

$J_B = x$

x \ AB	00	01	11	10
0	X	1	1	X
1	X	0	0	X

$K_B = x'$

Design Example - 4

Design Example - 4